Ver 1.1

14-Bit 120MSPS Digital to Analog Converter

Datasheet

Part Number：B9764MGRH

中国航天 CASC
北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2016.12	-	-	
1.1	2018.3	-	Changed the template	

TABLE OF CONTENTS

1. Features 1
2. Product Description 1
3. Function Block Dragram 2
4. Pin Description 2
5. Pin Definition（Appendix 1） 3
6. Product Application 3
6.1 Functional Description 3
6.1.1 DAC Transfer Function 5
6.1.2 Reference Operation 6
6.1.3 Reference Control Amplifier 7
6.1.4 Analog Inputs 10
6.1.5 Digital Inputs 12
6.1.6 Sleep Mode Operation 14
6.1.7 Power Dissipation 14
6.1.8 Output Configurations 14
6.1.9 Differential Coupling Using A Transformer 15
6.1.10 Differential Using An Op Amp 15
6.1.11 Single-Ended Unbuffered Voltage Output 16
6.1.12 Single-Ended Buffered Voltage Output Configuration 17
6.2.13 Power And Grounding Considerations 18
6.2 Absolute Maximum Ratings 19
6.3 Recommended Operating Conditions 19
6.4 Storage Condition 19
6.6 Radiation hardened performance 20
7. Electrical Specifications 20
8. Typical Application（Appendix 2） 23
9. Outline Dimensions 23
Appendix1. Pin Definition 25
Appendix2. Typical Application 26

1. Features

- 120MSPS Update Rate
- 14-Bit Resolution
- Excellent SFDR
- Differential Current Outputs: 2 mA to 20 mA
- Power Dissipation: 200 mW @ 5 V
- On-Chip 1.20 V Reference
- Single +5 V or +3.3 V Supply Operation
- Package: 28-Pin CPGA
- Edge-Triggered Latches
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV cm^2/mg

2. Product Description

The B9764MGRH is a radiation hardened, 14-bit resolution, high performance, low power CMOS digital-to-analog converters (DACs). It is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, providing an upward or downward component selection path based on performance, resolution and cost. The B9764MGRH offers exceptional ac and dc performance while supporting update rates up to 120 MSPS.

The B9764MGRH's flexible single-supply operating 5V or 3.3V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to a half with a slight degradation in performance by lowering the full-scale current output.

The B9764MGRH is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution.

The B9764MGRH is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 kΩ output impedance.

Differential current outputs are provided to support single ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer. The output voltage compliance range is 1.25V.

The on-chip reference and control amplifier are configured for maximum

accuracy and flexibility. The B9764MGRH can be driven by the on-chip reference or by a variety of external reference voltages. The internal control amplifier, which provides a wide (>10:1) adjustment span, allows the B9764MGRH full-scale current to be adjusted over a 2 mA to 20 mA range while maintaining excellent dynamic performance. Thus, the B9764MGRH may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

3. Function Block Dragram

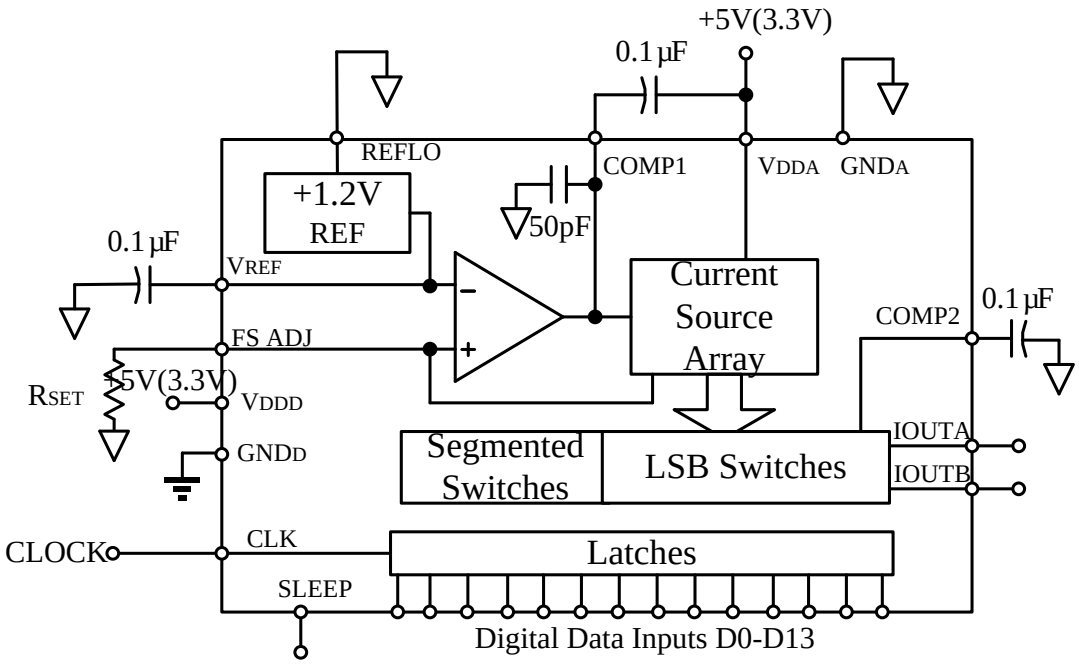


Figure 3-1, Function Block Diagram

4. Pin Description

CPGA28 Packaging,

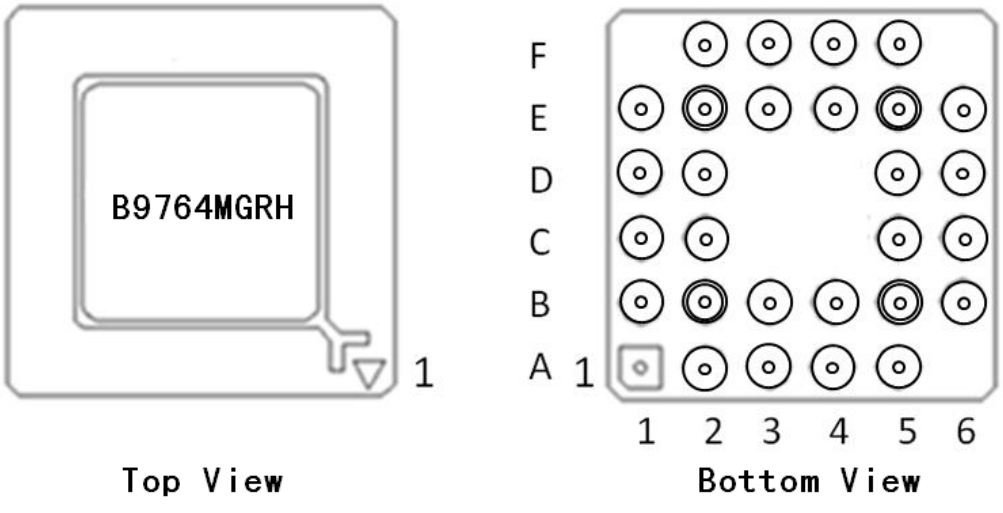


Figure 4-1, Pin Description

Table 4-1 B9764MGRH Pin Description

Symbol	Function Description
D0~13	Data Bits（LSB~MSB）
SLEEP	Power Down Control Input, HI：Sleep, LO：Normal
REFLO	Reference choose. 1) Connect to VDDA to disable internal reference . 2)Ground when Internal 1.2 V Reference Used.
V_{REF}	Reference Input/Output
FSADJ	Full-Scale Current Output Adjust
COMP1	Bandwidth/Noise Reduction Node. Add 0.1 mF to VDDA for optimum performance
GND_A	Analog Common.
IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
COMP2	Internal Bias Node for Switch Driver Circuitry. Decouple to GND with 0.1 mF capacitor
V_{DDA}	Analog Supply Voltage
GND_D	Digital Common.
V_{DDD}	Digital Supply Voltage
CLK	Clock Input. Data latched on positive edge of clock

Note：All input pins are should not float.

5. Pin Definition（Appendix 1）

6. Product Application

6.1 Functional Description

Figure 6-1 shows a simplified block diagram of the B9764MGRH. The B9764MGRH consists of a large PMOS current source array that is capable of providing up to 20mA of total current. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits or middle bits consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and

helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The digital section, which is capable of operating up to a 120 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.2V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2mA to 20mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference VREFIO, sets the reference current I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is 32 times the value of I_{REF}.

Figure 6-2 shows the relationship between Clock and Output.

Figure 6-2 shows the Basic AC Characterization Test Setup for B9764MGRH.

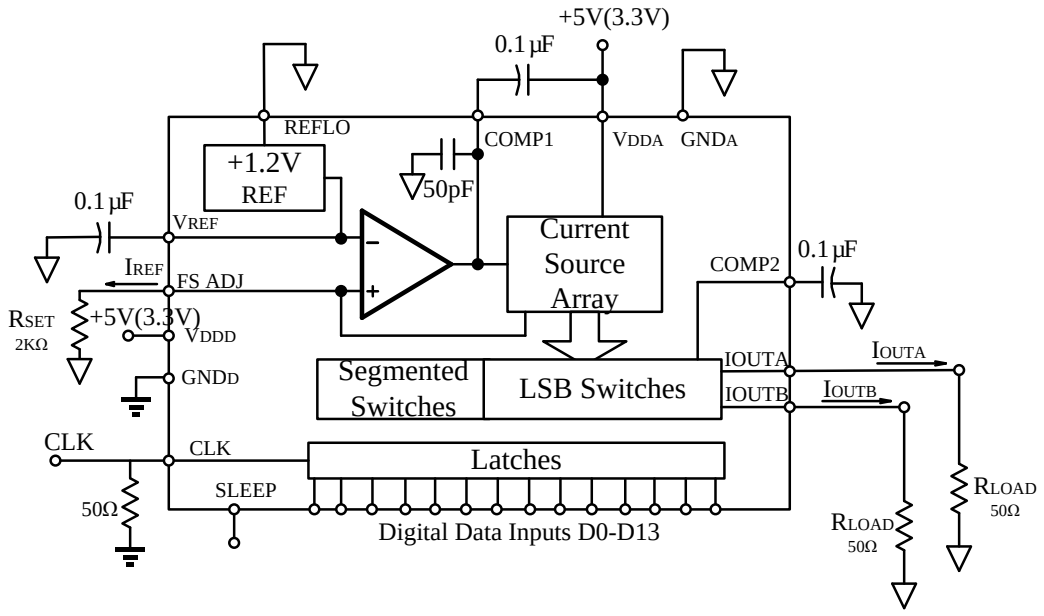


Figure 6-1. Simplified Block Diagram

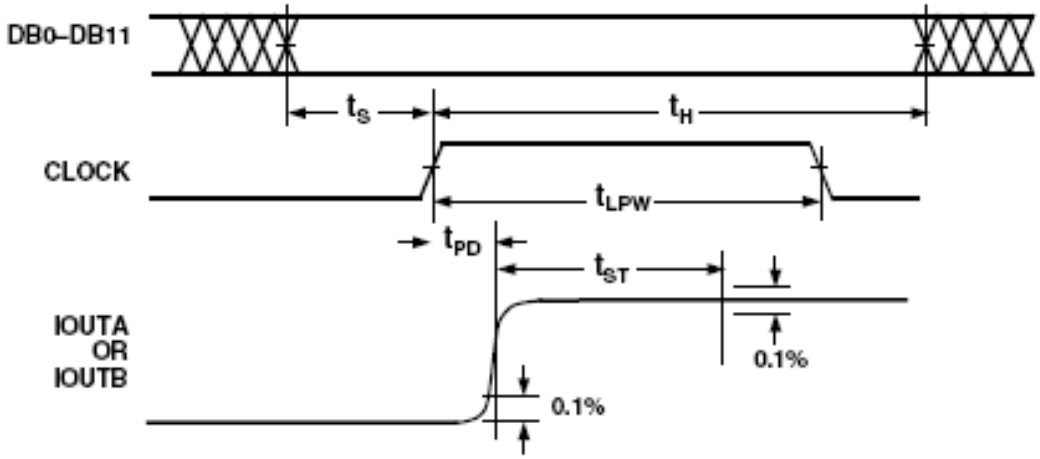


Figure 6-2 Timing of Output

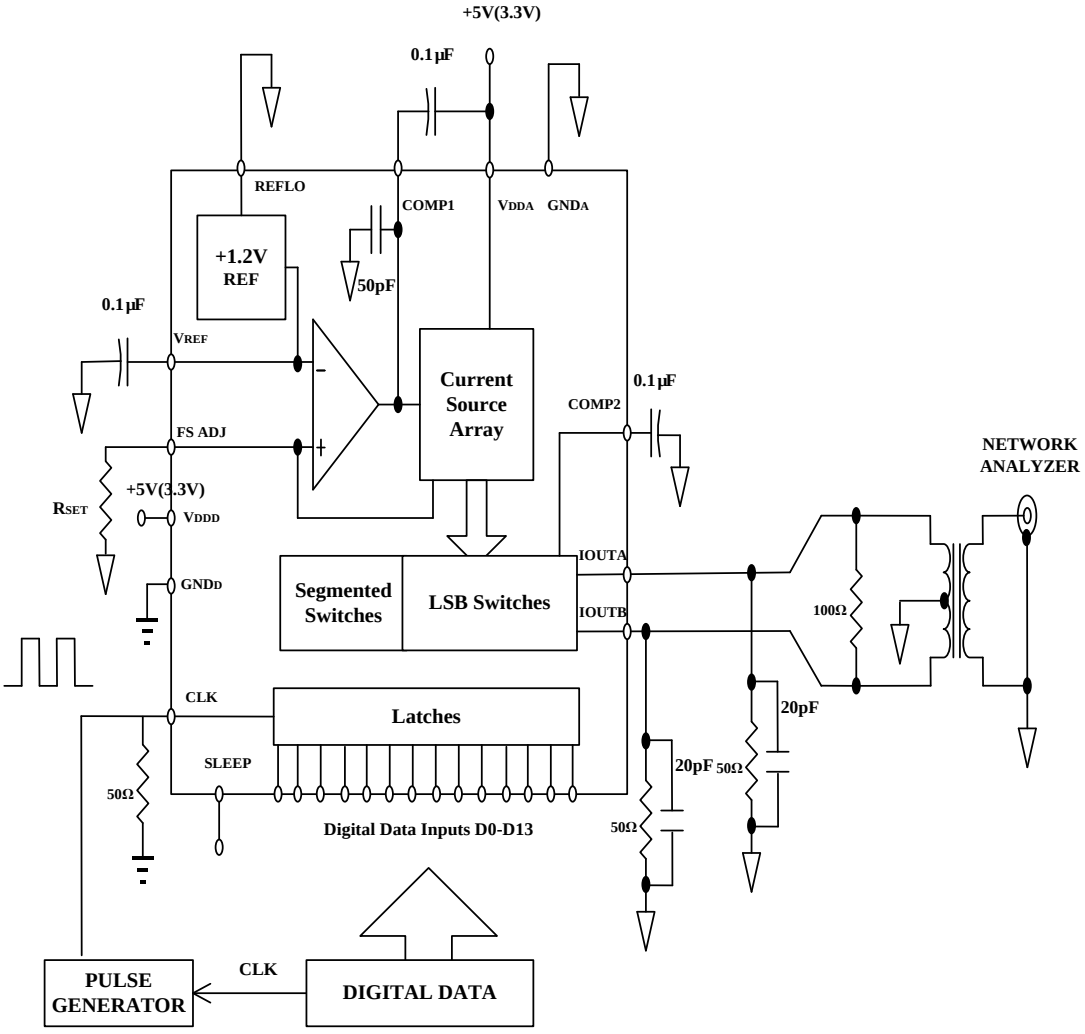


Figure 6-3. Basic AC Characterization Test Setup

6.1.1 DAC Transfer Function

The B9764MGRH provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, when all bits are high (i.e., DAC CODE =16383) while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as:

$$I_{OUTA}=(DACCODE/16384)\times I_{OUTFS} \quad (1)$$

$$I_{OUTB}=(16383-DACCODE)/16384\times I_{OUTFS} \quad (2)$$

Where DAC CODE = 0 to 16383 (i.e., Decimal Representation). As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REF} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS}=32\times I_{REF} \quad (3)$$

where：

$$I_{REF}=V_{REF}/R_{SET} \quad (4)$$

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, GND_A. Note that R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50Ω or 75Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply:

$$V_{OUTA}=I_{OUTA}\times R_{LOAD} \quad (5)$$

$$V_{OUTB}=I_{OUTB}\times R_{LOAD} \quad (6)$$

Note that the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

$$V_{DIFF}=(I_{OUTA}-I_{OUTB})\times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB} and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF}=\{(2\times DAC\ CODE-16383)/16384\}(32\times R_{LOAD}/R_{SET})\times V_{REF} \quad (8)$$

These last two equations highlight some of the advantages of operating the B9764MGRH differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion and dc offsets. Second, the differential code-dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note that the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the B9764MGRH can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

6.1.2 Reference Operation

The B9764MGRH contains an internal 1.2V bandgap reference that can be easily

disabled and overridden by an external reference. REFIO serves as either an input or output, depending on whether the internal or external reference is selected. If REFLO is tied to GND_A, as shown in Figure 6-4, the internal reference is activated, and V_{REF} provides a 1.2V output. In this case, the internal reference must be compensated externally with a ceramic chip capacitor of 0.1 uF or greater from V_{REF} to REFLO. Also, V_{REF} should be buffered with an external amplifier having an input bias current less than 100 nA if any additional loading is required.

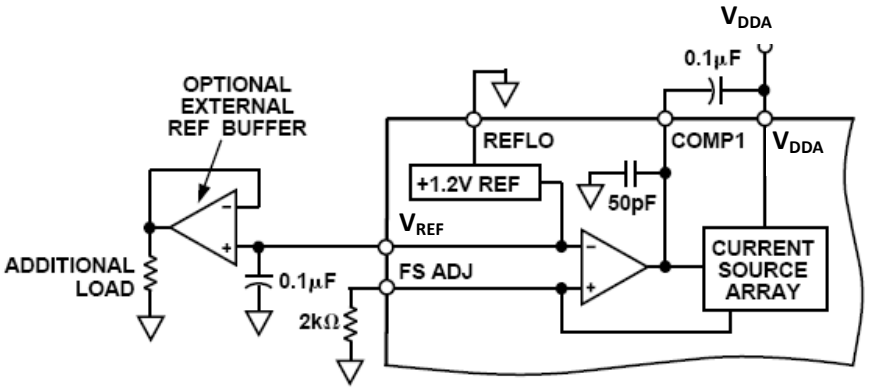


Figure 6-4. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to V_{DDA}. In this case, an external reference may then be applied to V_{REF} as shown in Figure 6-5. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1uF compensation capacitor is not required since the internal reference is disabled, and the high input impedance (i.e., 1MΩ) of V_{REF} minimizes any loading of the external reference.

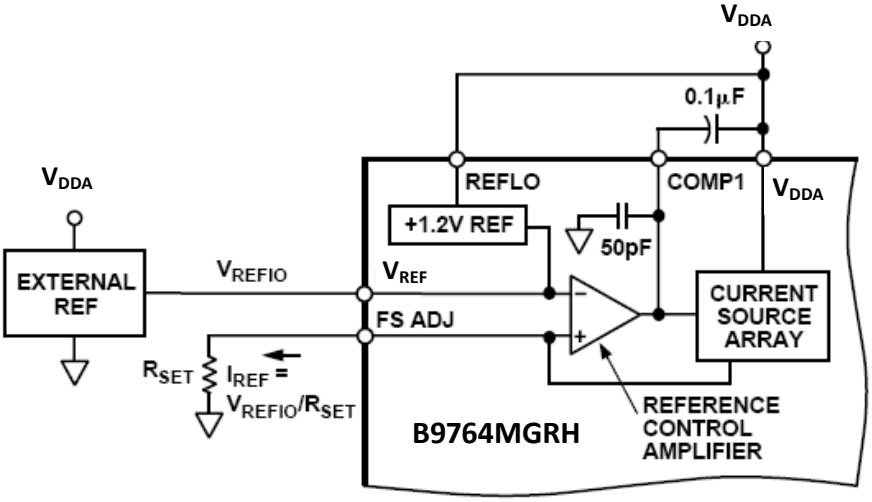


Figure 6-5. External Reference Configuration

6.1.3 Reference Control Amplifier

The B9764MGRH also contains an internal control amplifier that is used to

regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 6-5, such that its current output, I_{REF}, is determined by the ratio of the V_{REF} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied over to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide adjustment span of I_{OUTFS} over a 2mA to 20mA range by setting I_{REF} between 62.5uA and 625uA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the B9764MGRH, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 1.4 MHz and can be reduced by connecting an external capacitor between COMP1 and V_{DDA}. The output of the control amplifier, COMP1, is internally compensated via a 50pF capacitor that limits the control amplifier small-signal bandwidth and reduces its output impedance. Any additional external capacitance further limits the bandwidth and acts as a filter to reduce the noise contribution from the reference amplifier. Figure 6-6 shows the relationship between the external capacitor and the small signal –3dB bandwidth of the reference amplifier. Since the –3dB bandwidth corresponds to the dominant pole, and hence the time constant, the settling time of the control amplifier to a stepped reference input response can be approximated.

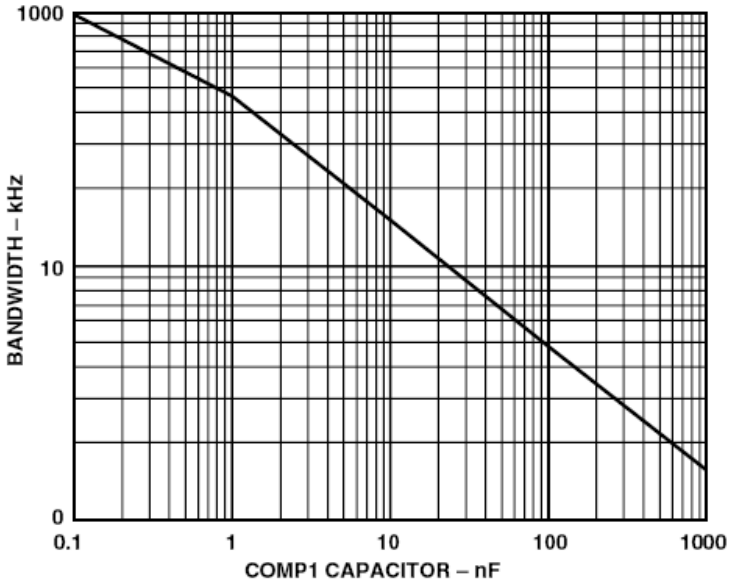


Figure 6-6. External COMP1 Capacitor vs. –3 dB Bandwidth

The optimum distortion performance for any reconstructed waveform is obtained with a 0.1uF external capacitor installed. Thus, if I_{REF} is fixed for an application, a 0.1uF ceramic chip capacitor is recommended. Also, since the control amplifier is optimized for low power operation, multiplying applications requiring large signal

swings should consider using an external control amplifier to enhance the application's overall large signal multiplying bandwidth and/or distortion performance.

There are two methods in which I_{REF} can be varied for a fixed R_{SET}. The first method is suitable for a single-supply system in which the internal reference is disabled, and the common-mode voltage of V_{REF} is varied over its compliance range of 1.25 V to 0.10 V. V_{REF} can be driven by a single-supply amplifier or DAC, thus allowing I_{REF} to be varied for a fixed R_{SET}. Since the input impedance of V_{REF} is approximately 1 MΩ, a simple, low cost R-2R ladder DAC configured in the voltage mode topology may be used to control the gain. This circuit is shown in Figure 6-7 using the AD7524 and an external 1.2 V reference, the AD1580.

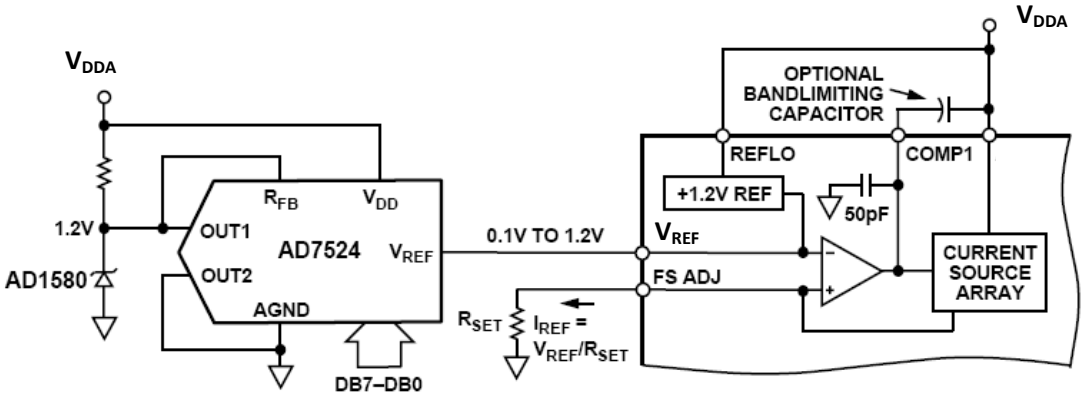


Figure 6-7. Single-Supply Gain Control Circuit

The second method may be used in a dual-supply system in which the common-mode voltage of V_{REF} is fixed, and I_{REF} is varied by an external voltage, V_{GC}, applied to R_{SET} via an amplifier. An example of this method is shown in Figure 6-8 in which the internal reference is used to set the common-mode voltage of the control amplifier to 1.2V. The external voltage, V_{GC}, is referenced to GND_A and should not exceed 1.2 V. The value of R_{SET} is such that I_{REFMAX} and I_{REFMIN} do not exceed 62.5uA and 625uA, respectively. The associated equations in Figure 26 can be used to determine the value of R_{SET}.

V_{DDA}

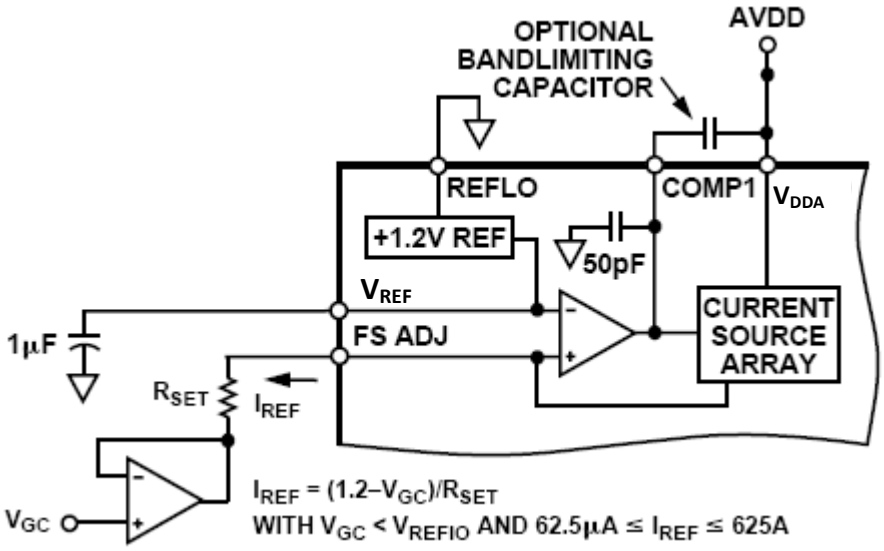


Figure 6-8. Dual-Supply Gain Control Circuit

In some applications, the user may elect to use an external control amplifier to enhance the multiplying bandwidth, distortion performance and/or settling time. External amplifiers capable of driving a 50 pF load such as the AD817 are suitable for this purpose. It is configured in such a way that it is in parallel with the weaker internal reference amplifier as shown in Figure 6-9. In this case, the external amplifier simply overdrives the weaker reference control amplifier. Also, since the internal control amplifier has a limited current output, it will sustain no damage if overdriven.

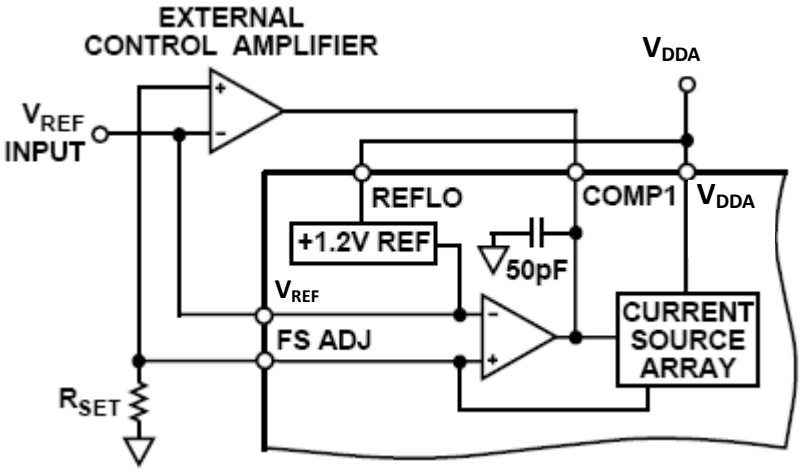


Figure 6-9. Configuring an External Reference Control Amplifier

6.1.4 Analog Inputs

The B9764MGRH produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which may be configured for single-end or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and

V_{OUTB} can also be converted to a single-ended voltage via a transformer or differential amplifier configuration.

Figure 6-10 shows the equivalent analog output circuit of the B9764MGRH consisting of a parallel combination of PMOS differential current switches associated with each segmented current source. The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches and is typically 100 kW in parallel with 5 pF. Due to the nature of a PMOS device, the output impedance is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) and, to a lesser extent, the analog supply voltage, V_{DDA}, and full-scale current, I_{OUTFS}. Although the output impedance's signal dependency can be a source of dc nonlinearity and ac linearity (i.e., distortion), its effects can be limited if certain precautions are noted.

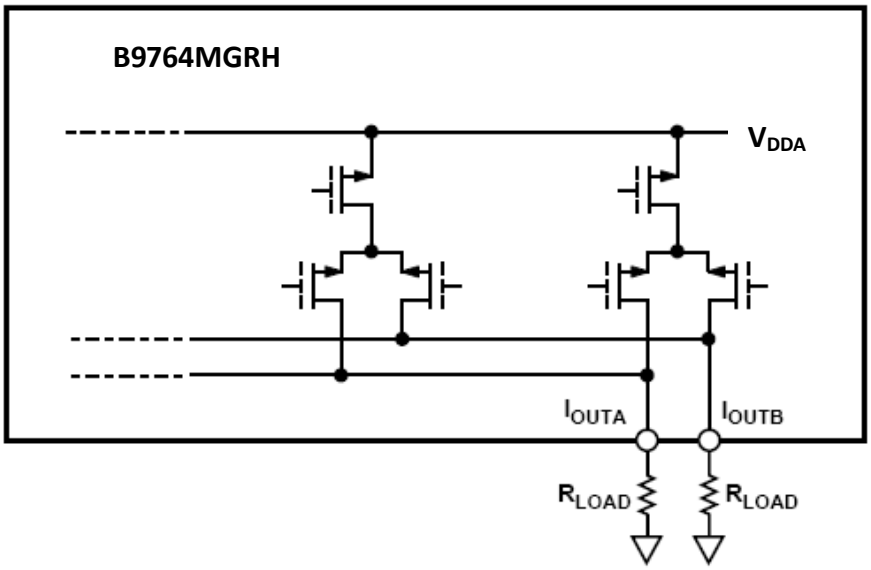


Figure 6-10. Equivalent Analog Output Circuit

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range. The negative output compliance range of –1V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the B9764MGRH. The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.2V for an I_{OUTFS} = 20mA to 1V for an I_{OUTFS} = 2 mA. Operation beyond the positive compliance range will induce clipping of the output signal which severely degrades the B9764MGRH's linearity and distortion performance.

Operating the B9764MGRH with reduced voltage output swings at I_{OUTA} and I_{OUTB} in a differential or single-ended output configuration reduces the signal dependency of its output impedance thus enhancing distortion performance. Although the voltage compliance range of I_{OUTA} and I_{OUTB} extends from –1.0 V to +1.2V,

optimum distortion performance is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed approximately 0.5 V. A properly selected transformer with a grounded center-tap will allow the B9764MGRH to provide the required power and voltage levels to different loads while maintaining reduced voltage swings at I_{OUTA} and I_{OUTB}. DC-coupled applications requiring a differential or single-ended output configuration should size R_{LOAD} accordingly. Refer to Applying the B9764MGRH section for examples of various output configurations.

The most significant improvement in the B9764MGRH's distortion and noise performance is realized using a differential output configuration. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be substantially reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include evenorder distortion products and noise. The enhancement in distortion performance becomes more significant as the reconstructed waveform's frequency content increases and/or its amplitude decreases.

For applications requiring the optimum dc linearity, I_{OUTA} and/or I_{OUTB} should be maintained at a virtual ground via an I-V op amp configuration. Maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground keeps the output impedance of the B9764MGRH fixed, significantly reducing its effect on linearity. However, it does not necessarily lead to the optimum distortion performance due to limitations of the I-V op amp. Note that the INL/DNL specifications for the B9764MGRH are measured in this manner using I_{OUTA}.

6.1.5 Digital Inputs

The B9764MGRH's digital input consists of 14 data input pins and a clock input pin. The 14-bit parallel data inputs follow standard positive binary coding where DB13 is the most significant bit (MSB), and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at logic 1. I_{OUTB} produces a complementary output with the fullscale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch. The DAC output is updated following the rising edge of the clock as shown in Figure 1 and is designed to support a clock rate as high as 120 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulse width. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

The digital inputs are CMOS-compatible with logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (V_{DDD}) or

$$V_{THRESHOLD}=V_{DDD}/2(\pm 20\%)$$

The internal digital circuitry of the B9764MGRH is capable of operating over a digital supply 5V or 3.3V. As a result, the digital inputs can also accommodate TTL levels when V_{DDD} is set to accommodate the maximum high level voltage of the TTL drivers VOH(MAX). Figure 6-11 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar with the exception that it contains an active pull-down circuit, thus ensuring that the B9764MGRH remains enabled if this input is left disconnected.

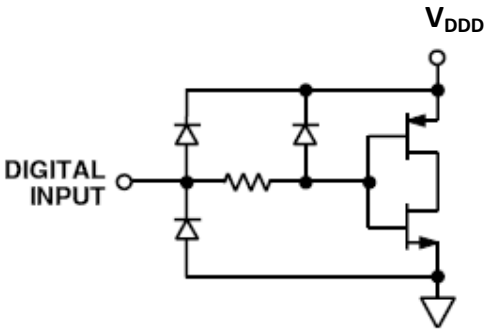


Figure 6-11. Equivalent Digital Input

Since the B9764MGRH is capable of being updated up to 120MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. Operating the B9764MGRH with reduced logic swings and a corresponding digital supply (V_{DDD}) will result in the lowest data feedthrough and on-chip digital noise. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the B9764MGRH as well as its required min/max input logic level thresholds.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20Ω to 100 Ω) between the B9764MGRH digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain “clean” digital inputs.

The external clock driver circuitry should provide the B9764MGRH with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

Note, that the clock input could also be driven via a sine wave, which is centered around the digital threshold (i.e., V_{DDD} /2) and meets the min/max logic threshold. This will typically result in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Also, at higher

sampling rates, the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and, subsequently, cut into the required data setup and hold times.

6.1.6 Sleep Mode Operation

The B9764MGRH has a power-down function that turns off the output current and reduces the supply current to less than 8.5 mA over the specified supply 5V or 3.3V and temperature range. This mode can be activated by applying a logic level "1" to the SLEEP pin. This digital input also contains an active pull-down circuit that ensures the B9764MGRH remains enabled if this input is left disconnected.

The power-up and power-down characteristics of the B9764MGRH are dependent upon the value of the compensation capacitor connected to COMP1. With a nominal value of 0.1 uF, the B9764MGRH takes less than 5 us to power down and approximately 3.25 ms to power back up. Note, the SLEEP MODE should not be used when the external control amplifier is used .

6.1.7 Power Dissipation

The power dissipation, PD, of the B9764MGRH is dependent on several factors, including: (1) V_{DDA} and V_{DDD}, the power supply voltages; (2) I_{OUTFS}, the full-scale current output; (3) f_{CLOCK}, the update rate; and (4) the reconstructed digital input waveform.

6.1.8 Output Configurations

The following sections illustrate some typical output configurations for the B9764MGRH. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor, R_{LOAD}, referred to GND_A. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since I_{OUTA} or I_{OUTB} is maintained at a virtual ground. Note, I_{OUTA} provides slightly better performance than I_{OUTB}.

6.1.9 Differential Coupling Using A Transformer

An RF transformer can be used to perform a differential-tosingle- ended signal conversion as shown in Figure 6-12. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

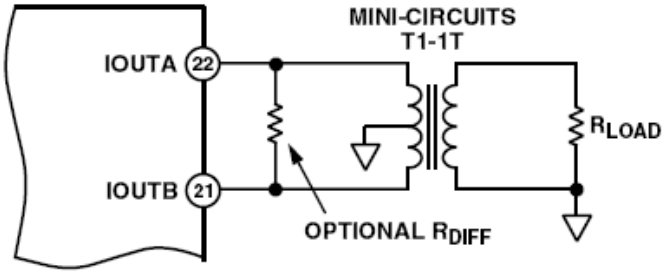


Figure 6-12. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to GND_A to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around GND_A and should be maintained with the specified output compliance range of the B9764MGRH. A differential resistor, R_{DIFF}, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

6.1.10 Differential Using An Op Amp

An op amp can also be used to perform a differential-to-singleended conversion as shown in Figure 6-13. The B9764MGRH is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DAC's high slewing output from overloading the op amp's input.

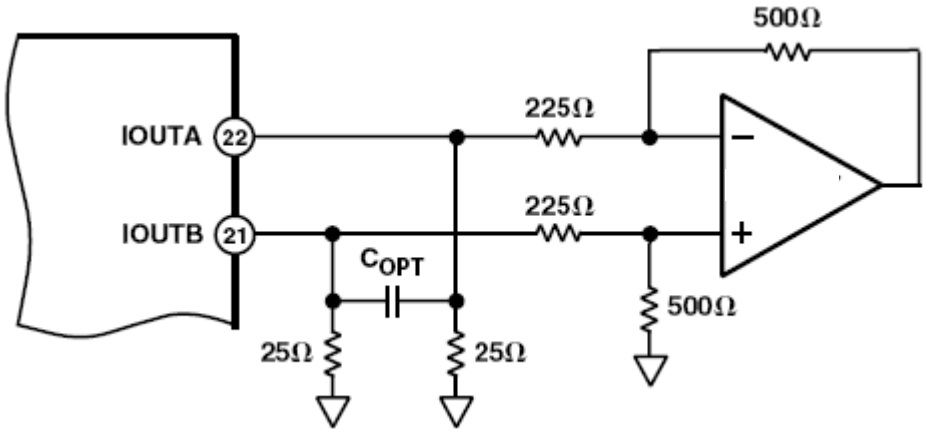


Figure 6-13. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit is configured to provide some additional signal gain. The op amp must operate from a dual supply since its output is approximately ±1V. A high speed amplifier capable of preserving the differential performance of the B9764MGRH while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 6-14 provides the necessary level-shifting required in a single supply system. In this case, V_{DDA}, which is the positive analog supply for both the B9764MGRH and the op amp, is also used to level-shift the differential output of the B9764MGRH to midsupply (i.e., $V_{DDA}/2$).

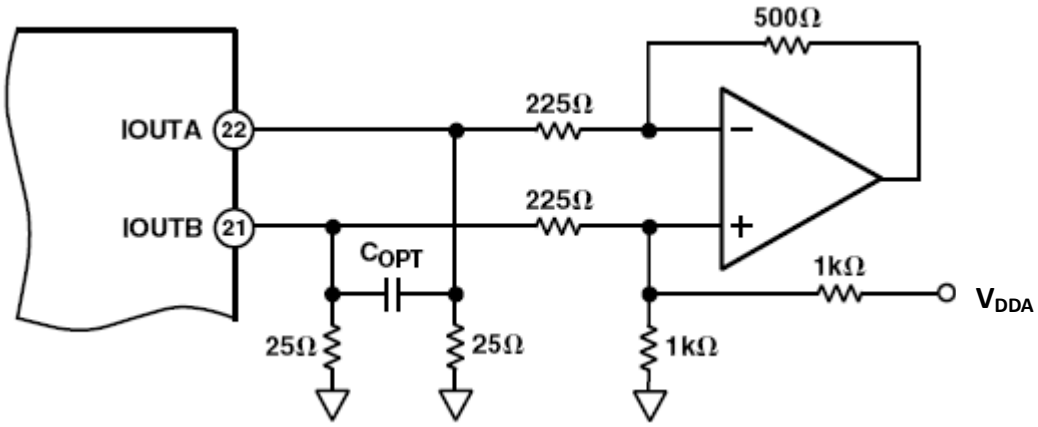


Figure6-14. Single-Supply DC Differential Coupled Circuit

6.1.11 Single-Ended Unbuffered Voltage Output

Figure 6-15 shows the B9764MGRH configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent RLOAD of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or

I_{OUTB}. The unused output (I_{OUTA} or I_{OUTB}) can be connected to GND_A directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the Analog Output section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

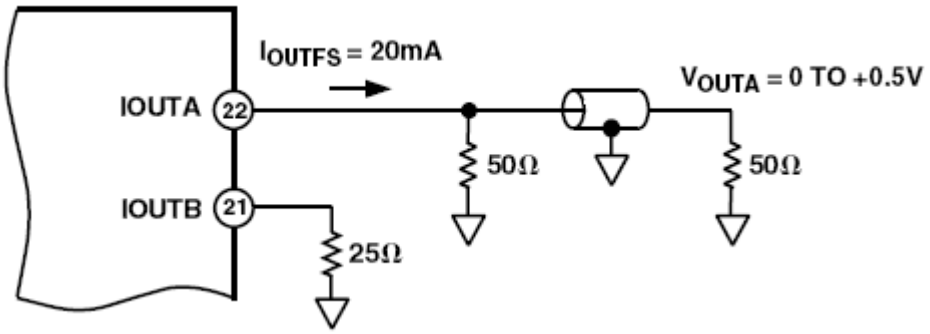


Figure 6-15. 0 V to +0.5 V Unbuffered Voltage Output

6.1.12 Single-Ended Buffered Voltage Output Configuration

Figure 6-16 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the B9764MGRH output current. U1 maintains I_{OUTA} (or I_{OUTB}) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the Analog Output section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of RFB and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or RFB. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

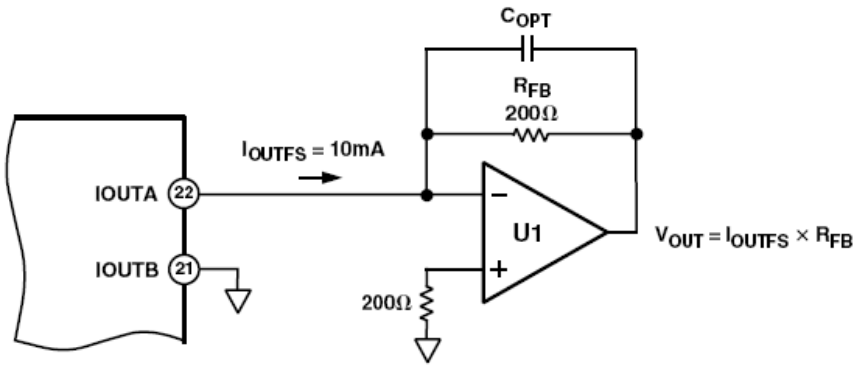


Figure 6-16. Unipolar Buffered Voltage Output

6.1.13 Power And Grounding Considerations

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection, placement and routing and supply bypassing and grounding.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The B9764MGRH features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, V_{DDA}, the analog supply, should be decoupled to GND_A, the analog common, as close to the chip as physically possible. Similarly, V_{DDD}, the digital supply, should be decoupled to GNDD as close as physically as possible.

For those applications requiring a single +5V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 6-17. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

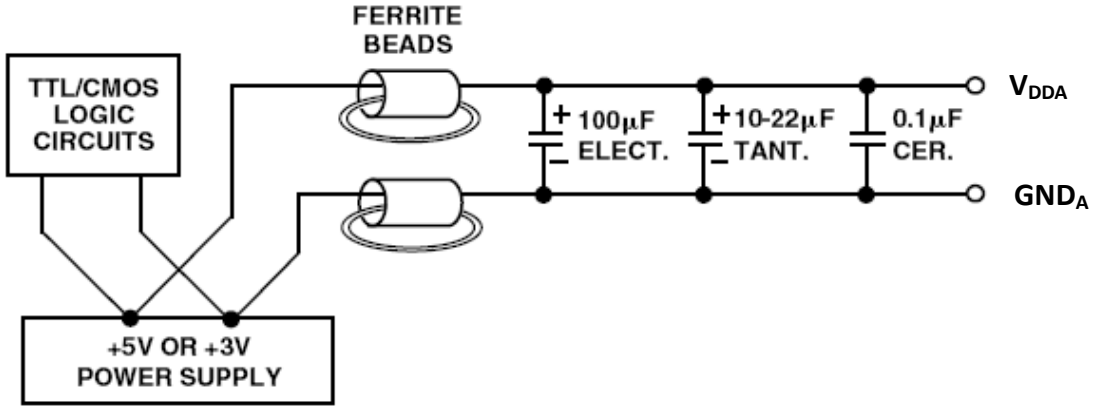


Figure 6-17. Differential LC Filter for Single +5 V or +3 V Applications

Maintaining low noise on power supplies and ground is critical to obtain optimum results from the B9764MGRH. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane

is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as providing some "free" capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct and as physically close to the package as possible in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistors should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

6.2 Absolute Maximum Ratings

1) Power Supply (V_{DDD},V_{DDA}) ..... -0.3V~6.5 V
2) Digital Input Voltage（V_{ID}）..... -0.3V~V_{DDD}+0.3V
3) Analog Input/Output Voltage（V_{IA}、V_{OA}）..... -0.3V~V_{DDA}+0.3V
4) Input Reference Voltage（V_{REF}）..... 0.2V~1.25V
5) I_{OUTA},I_{OUTB} Output Voltage（V_{IOUTA}、V_{IOUTB}）..... -1.0V~1.25V
6） Storage Temperature(T_{STG}) .....-65℃~+ 150℃
7) Lead Temperature(10s)(T_h) .....260℃（MAC），300℃（Manual）
8) Thermal Resistance(θJC) ..... 20℃/W
9) Junction Temperature (TJ) ..... 175℃

6.3 Recommended Operating Conditions

1) Power Supply（V_{DDD},V_{DDA}）..... 3.15V~5.25V
2) Output Resistance 50Ω
3) Operating Range（T_A）..... -55℃~125℃

6.4 Storage Condition

The warehouse environment of B9764MGRH should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

Table 6-1. The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

6.5 Radiation hardened performance

a) Total Ionizing Dose ≥ 100 Krad(Si)

b) SEL threshold ≥ 75 MeV cm^2/mg

7. Electrical Specifications

-55℃≤T_A≤125℃,, unless otherwise specified.

Table 7-1. Electronic Specifications

Parameter	Symbol	Condition (V_{DDD}=V_{DDA}=5V) Io=20mA -55℃ ≤ T_A ≤ 125℃	Data			Unit
			Min	Typ	Max	
INL	E_L	V_{DDD}=V_{DDA} =5V	-6.5	—	+6.5	LSB
		V_{DDD}=V_{DDA} =3.3V	-8.5	—	+8.5	
DNL	E_{DL}		-4.5	—	+4.5	LSB
Offset Error	E_O	Internal Reference(T_A=25℃)	-0.1	—	+0.1	%FS
Gain Error	E_G	Internal Reference (T_A=25℃)	-10.0	—	+10.0	%FS
Reference Output Voltage	V_{REF}		1.08	—	1.32	V
Digital input capacitance	C_{IN}		—	6	—	pF
Analog output resistance	R_{OUT}		—	104	—	kΩ
Analog output capacitance	C_{OUT}		—	11	—	pF
Reference input resistance	R_{REF}		—	1.2	—	MΩ
Reference output current	I_{REF}		—	92	—	nA
Full-scale output current	I_{OUTFS}		2.0		20.0	mA
Digital Inputs Logic 1 Voltage	V_{IH}	V_{DDD}=V_{DDA} =5V	3.5	—	—	V
		V_{DDD}=V_{DDA} =3.3V	2.4	—	—	
Digital Inputs Logic 0 Voltage	V_{IL}	V_{DDD}=V_{DDA} =5V	—	—	1.3	V
		V_{DDD}=V_{DDA} =3.3V	—	—	0.8	
Digital Inputs Logic 1 Current	I_{IH}	V_I= V_{DDD}	-10.0	—	10.0	μA
Digital Inputs Logic 1 Current	I_{IL}	V_I=0V	-10.0	—	10.0	μA

Parameter	Symbol	Condition (V_{DDD}=V_{DDA}=5V) Io=20mA -55℃ ≤ T_A ≤ 125℃		Data			Unit
				Min	Typ	Max	
Analog Power Supply Rejection Ratio	$PSRR_{DDA}$	±5% Power Supply，V_{DDD}= 5V		-0.4	—	+0.4	%FSR/V
		±5% Power Supply，V_{DDD}= 3.3V		-1.0	—	+1.0	
Digital Power Supply Rejection Ratio	$PSRR_{DDD}$	±5% Power Supply，V_{DDD}= 5V		-0.1	—	+0.1	%FSR/V
		±5% Power Supply，V_{DDD}= 3.3V		-0.2	—	+0.2	
Offset Drift (TEMPERATURE)	α_{EO}			-0.02	—	+0.02	%FS/℃
Gain Drift (TEMPERATURE)	α_{EG}			-0.1	—	+0.1	%FS/℃
Reference Voltage Drift (TEMPERATURE)	α_{VREF}			-0.0002	—	+0.0002	1/℃
Analog Supply Current	I_{DDA}	R_{Load} = 50Ω		—	—	35.0	mA
Digital Supply Current	I_{DDD}	R_{Load} = 50Ω，f_{CLK}=25MSPS f_O=1.0MSPS		—	—	10.0	mA
Power Dissipation	P_W	R_{Load} = 50Ω， f_{CLK} =25MSPS fO =1.0MSPS		—	—	200	mW
SPURIOUS-FREE DYNAMIC RANGE	*SFDR*	V_{DDD}=V_{DDA} =5V	f_{CLK} =25MHz，f_O =1MHz,	66.0	—	—	dBc
			f_{CLK} =50MHz，f_O,=1MHz,	66.0	—	—	dBc
			f_{CLK} =50MHz，f_O =2MHz,	60.0	—	—	dBc
			f_{CLK} =60MHz，f_O =1MHz,	66.0	—	—	dBc
			f_{CLK} =100MHz，f_O =1MHz,	65.0	—	—	dBc
			f_{CLK} =120MHz，f_O=1MHz,	*63.0*	—	—	dBc
		V_{DDD}=V_{DDA} =3.3V	f_{CLK} =25MHz，f_O =1MHz,	65.0	—	—	dBc
			f_{CLK} =50MHz，f_O,=1MHz,	65.0	—	—	dBc

Parameter	Symbol	Condition (V_{DDD}=V_{DDA}=5V) Io=20mA -55℃ ≤ T_A ≤ 125℃		Data			Unit
				Min	Typ	Max	
			f_{CLK} =50MHz, f_O =2MHz,	58.0	—	—	dBc
			f_{CLK} =60MHz, f_O =1MHz,	63.0	—	—	dBc
			f_{CLK} =100MHz, f_O =1MHz,	63.0	—	—	dBc
			f_{CLK} =120MHz, f_O=1MHz,	*62.0*	—	—	dBc
TOTAL HARMONIC DISTORTION	*THD*	V_{DDD}=V_{DDA} =5V	f_{CLK} =25MHz, f_O =1MHz,	—	—	-64.0	dBc
			f_{CLK} =50MHz, f_O,=1MHz,	—	—	-64.0	dBc
			f_{CLK} =50MHz, f_O =2MHz,	—	—	-58.0	dBc
			f_{CLK} =60MHz, f_O =1MHz,	—	—	-63.0	dBc
			f_{CLK} =100MHz, f_O =1MHz,	—	—	-62.0	dBc
			f_{CLK} =120MHz, f_O=1MHz,	—	—	*-62.0*	dBc
		V_{DDD}=V_{DDA} =3.3V	f_{CLK} =25MHz, f_O =1MHz,	—	—	-62.0	dBc
			f_{CLK} =50MHz, f_O,=1MHz,	—	—	-61.0	dBc
			f_{CLK} =50MHz, f_O =2MHz,	—	—	-56.0	dBc
			f_{CLK} =60MHz, f_O =1MHz,	—	—	-61.0	dBc
			f_{CLK} =100MHz, f_O =1MHz,	—	—	-61.0	dBc

Parameter	Symbol	Condition (V_{DDD}=V_{DDA}=5V） Io=20mA -55℃ ≤ T_A ≤ 125℃		Data			Unit
				Min	Typ	Max	
			f_{CLK} =120MHz， f_O=1MHz,	—	—	*-60.0*	dBc
Output Setup Time	t_{su}			—	—	50.0	ns
Digital input Setup Time	t_S			2.0	—	—	ns
Digital input Hold Time	t_H			2.0	—	—	ns
Clock Pulse Width	t_{LPW}			4.5	—	—	ns
Output rise time (10% to 90%)	t_U			—	6	—	ns
Output fall time (10% to 90%)	t_D			—	8	—	ns
Output delay	t_{pD}			—	6	—	ns
Maximum Frequency	f_{max}			100.0	—	—	MHz

8. Typical Application（Appendix 2）

9. Outline Dimensions

CPGA28 Packaging.

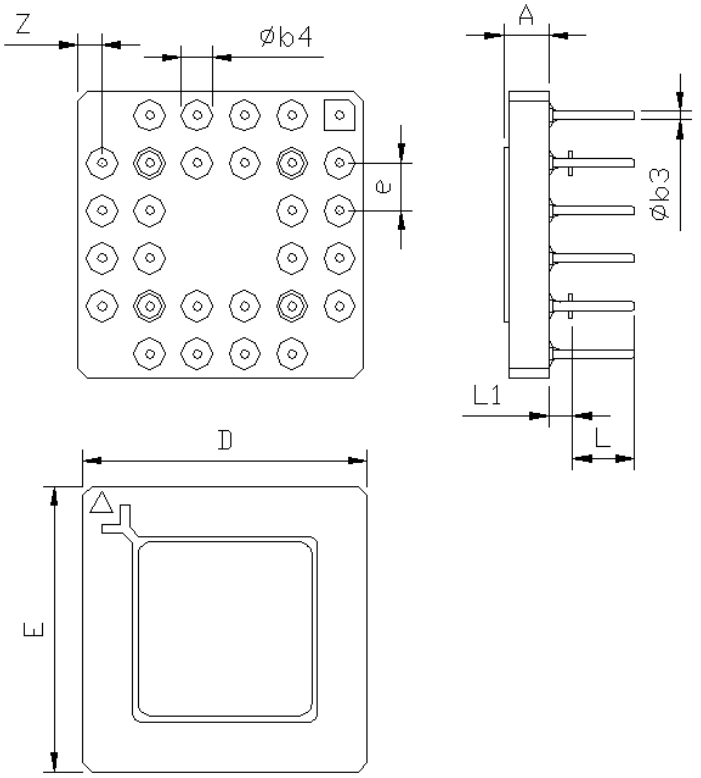


Figure 9-1. B9764MGRH's Packaging(CPGA28)

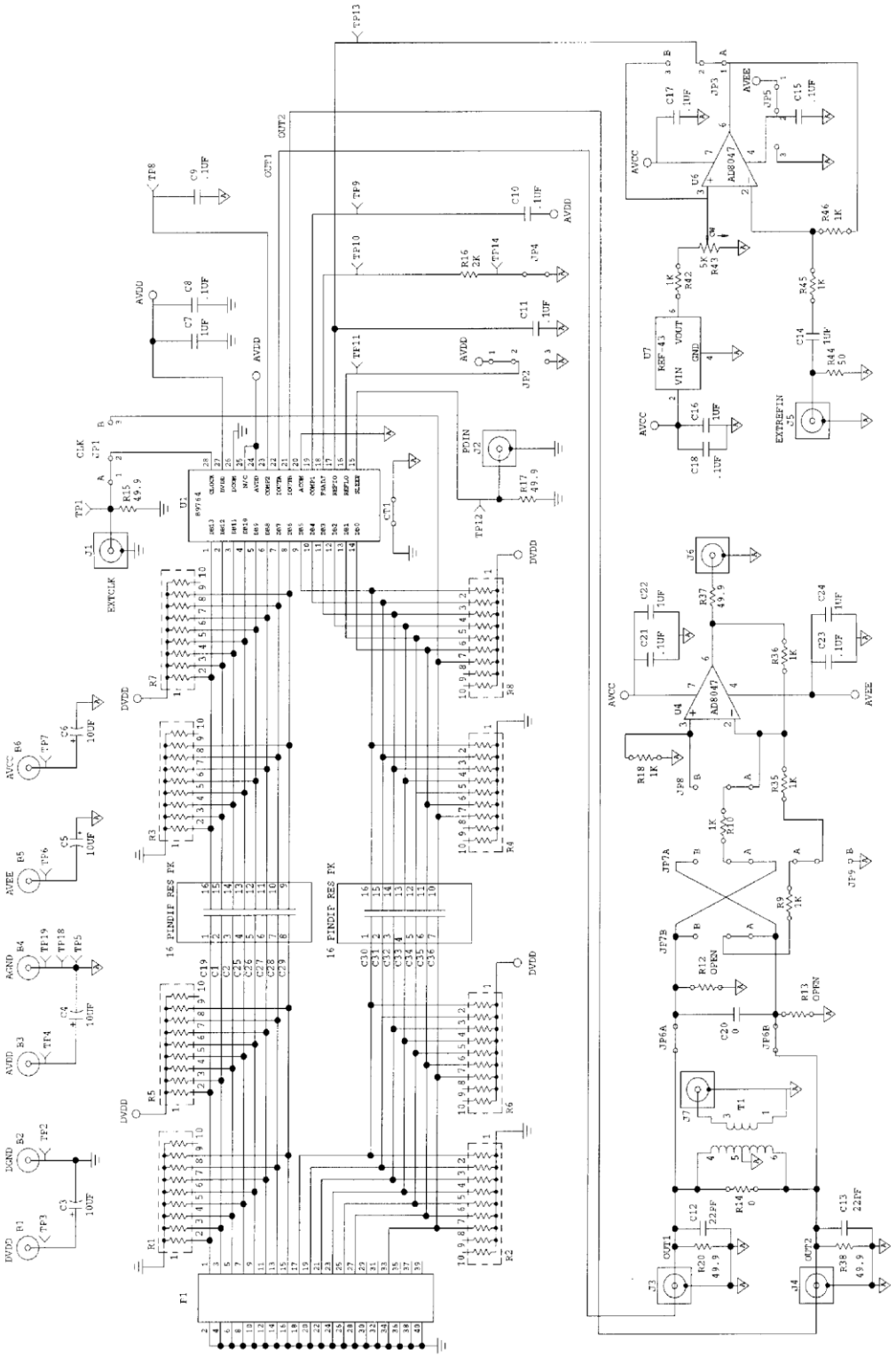
Symbol	Values(Units:mm)		
	Min.	Typ.	Max.
D	15.09	——	15.39
E	15.09	——	15.39
Z	——	1.27	——
A	1.78	——	3.68
e	——	2.54	——
L1	1.02	——	1.52
L	2.54	——	5.08
Φb3	0.41	——	0.51
Φb4	1.50	——	1.80

Appendix1. Pin Definition

Appendix Table1-1 Pin Definition

Pin	Symbol	Type	Description	Pin	Symbol	Type	Description
A3	D13	I	Most Significant Data Bit (MSB)	F4	SLEEP	I	Power-Down Control Input. Active High. Contains active pull-down circuit; it may be left unterminated if not used
B3	D12	I	Data Bit 12	E4	REFLO	I	Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference
A2	D11	I	Data Bit 11	F5	V_{REF}	I /O	Reference Input/Output
B2	D10	I	Data Bit 10	E5	FSADJ	I	Full-Scale Current Output Adjust
B1	D 9	I	Data Bit 9	E6	COMP1	I	Bandwidth/Noise Reduction Node. Add 0.1 mF to AVDD for optimum performance
C2	D8	I	Data Bit 8	D5	GND_A	G	Analog Common
C1	D7	I	Data Bit 7	D6	IOUTB	O	Complementary DAC Current Output. Full-scale current when all data bits are 0s
D1	D6	I	Data Bit 6	C6	IOUTA	O	DAC Current Output. Full-scale current when all data bits are 1s
D2	D5	I	Data Bit 5	C5	COMP2	O	Internal Bias Node for Switch Driver Circuitry. Decouple to ACOM with 0.1 mF capacitor
E1	D4	I	Data Bit 4	B6	V_{DDA}	P	Analog Supply Voltage
E2	D3	I	Data Bit 3	B5	NC	NC	No Internal Connection
F2	D2	I	Data Bit 2	A5	GND_D	G	Digital Common
E3	D1	I	Data Bit 1	B4	V_{DDD}	P	Digital Supply Voltage
F3	D0	I	Least Significant Data Bit （LSB）	A4	CLK	I	Clock Input. Data latched on positive edge of clock

Appendix2. Typical Application



Appendix Figure 2-1. Evaluation Board Schematic

Service & Supply

Address：No.2.Siyingmen N.Rd.Donggaodi, Fengtai District, Beijing, PRC

Department：Department of international cooperation

Telephone：+86(0)10-68757343

Email：gjhz@mxtronics.com

Fax：+86(0)10-68757706

Zip code：100076