Ver 1.0

Radiation-Hardened PROM

Datasheet

Part Number： B28F1024RH

中国航天 北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2018.4		Document creation	

TABLE OF CONTENTS

1. Features

- 1Mbit radiation-hardened asynchronous PROM, extended production of B28F256RH
- Configurations including 32Kx32bit, 64Kx16bit and 128Kx8bit
- Required to be programmed by the special programmer
- 50 ns maximum access time (-55°C ~ 125°C)
- TTL compatible inputs and TTL/CMOS compatible outputs levels, three-state bidirectional data bus
- Voltage supply: 4.5V ~ 5.5V
- ESD protect ≥ 2000 V
- Operational environment:
  Total-dose: 100 K Rad (Si)
  SEL: > 75 MeV·cm^2/mg
  SEU (Logic): > 37 MeV·cm^2/mg
  SEU (Memory Cell): > 75 MeV·cm^2/mg
- Packaging options: QFP64

2. General Description

The B28F1024RH PROM is a high performance, asynchronous, radiation-hardened, 1Mbit programmable memory device. The B28F1024RH PROM features fully asynchronous operation requiring no external clocks or timing strobes. B28F1024RH needs to be programmed by the special programmer. The combination of radiation-hardness, fast access time, and low power consumption make the B28F1024RH ideal for high speed systems designed for operation in radiation environments. It also can be off-chip PROM of systems, such as 80C32, 3803, DSP.

3. Pin Description

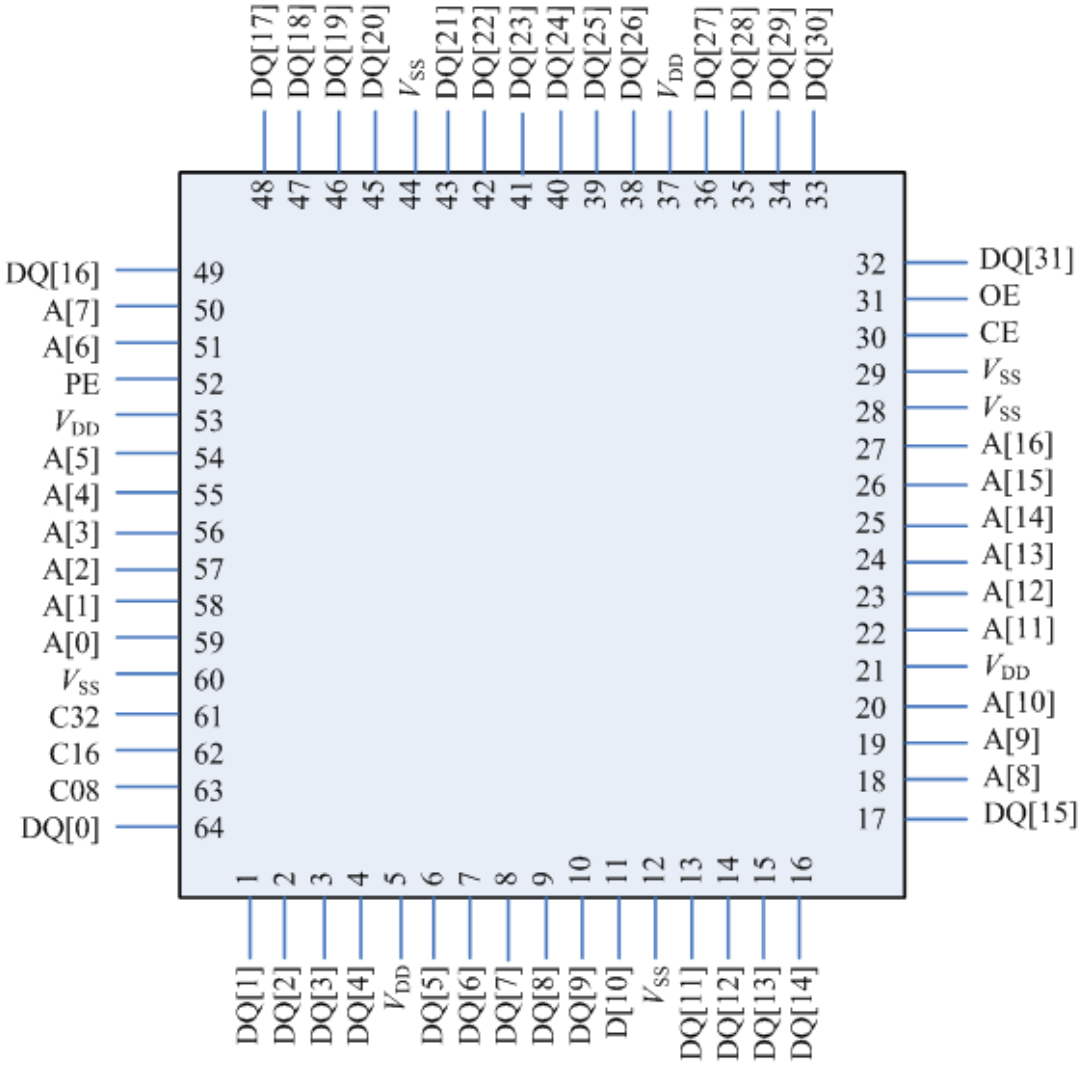


Figure 1 B28F1024RH PROM Pin Figuration

Table 1. Pin Names

Pin Names	Functions
C06 C16 C32	Selection signal of data bits width (active high)
A0~A16	Address
DQ0~DQ31	Data Input / Output
$\overline{CE}$	Chip Enable (Active Low)

$\overline{PE}$	Program Enable (Active Low)
$\overline{OE}$	Output Enable (Active Low)
V_{DD}	Power (5 V)
V_{SS}	Ground

4. Pin Configurations（Appendix 1）

5. Product Description

5.1 Function Description

The B28F1024RH has three control inputs: Chip Enable ($\overline{CE}$), Program Enable ($\overline{PE}$), and Output Enable ($\overline{OE}$); Selection signal of data bits width including C08, C16, C32; 17 address inputs, A(16:0); and 32 bidirectional data lines, DQ(31:0). $\overline{CE}$ is the device enable input that controls active and standby modes. Asserting $\overline{CE}$ causes the decode of the address inputs and the corresponding data in the memory is selected. $\overline{PE}$ controls program and read operations. During a read cycle, $\overline{OE}$ must be asserted to enable the outputs. The device can be configured into three states including 32Kx32bit, 64Kx16bit and 128Kx8bit.

If $\overline{CE}$=0, PE=1 and there is only one to keep high level among C08, C16 and C32, the other two keep low level and the device is in the read state of TMR(Triple Modular Redundancy). When C08=1, C16=0, C32=0, the device is in 128Kx8bit configuration, the data width of output is 8 and the high 24 bits are 0. When C08=0, C16=1, C32=0, the device is in 64kx16bit configuration, the data width of output is 16, and the high 16 bits are 0. When C08=0, C16=0, C32=1, the device is in 32Kx32bit configuration and the data width of output is 32.

Table 2. Device Operation Truth Table

Operation	$\overline{OE}$	$\overline{CE}$	$\overline{PE}$	C08	C16	C32	DQ
Stand by	X[1]	1	1	Only one of the three signals is 0.			3-state
8bit read	0	0	1	1	0	0	Data out
8bit read (data invalid)	1	0	1	1	0	0	3-state
16bit read	0	0	1	0	1	0	Data out
16bit read (data invalid)	1	0	1	0	1	0	3-state
32bit read	0	0	1	0	0	1	Data out
32bit read (data invalid)	1	0	1	0	0	1	3-state
programming	1	0	0	0	0	0	Data in
1、X=don't care.							

Notes:

1. The other combinations of $\overline{CE}$, $\overline{PE}$, $\overline{OE}$, C08, C16 and C32 which are not listed in the table are not allowed.
2. After programming, there is only one high level among C08, C16 and C32. The other two are both low levels.

◆ **Read Cycle**

A combination of $\overline{PE}$ greater than V_{IH}(min) and $\overline{CE}$ less than V_{IL}(max) defines a read cycle. For PROM, there are three control modes including address Access, chip enable controlled access and output enable controlled access.

Read Cycle 1, the Address Access in Figure 2, is initiated by a change in address inputs while the chip is enabled with $\overline{OE}$ asserted and $\overline{PE}$ deasserted. Valid data appears on data outputs after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

Read Cycle 2, the Chip Enable-controlled Access in Figure 3, is initiated by $\overline{CE}$ going active while $\overline{OE}$ remains asserted, $\overline{PE}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the data addressed by the input addresses is accessed and appears at the data outputs DQ.

Read Cycle 3, the Output Enable-controlled Access in Figure 4, is initiated by $\overline{OE}$ going 0 while $\overline{PE}$ is 1, $\overline{OE}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

5.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD}	Positive supply voltage	4.5 V ~ 5.5 V
T_C	Case temperature range	-55℃ ~ +125℃
V_I	DC input voltage	0 V ~ V_{DD}

$\overline{PE}$ should be tied to V_{DD} when the device is used.

6. Electrical Characteristics

6.1 DC Electrical Characteristics (Pre and Post-Radiation)

Table 4. DC Parameter Table

Parameter	Symbol	Condition -55°C≤T≤125°C; 4.5V≤V_{DD}≤5.5V	Limits		UNIT
			MIN	MAX	
High-level output voltage	V_{OH1}	V_{DD}=4.5V, I_{OH}= -100μA（CMOS）	V_{DD}-0.1	—	V
	V_{OH2}	V_{DD}=4.5V, I_{OH}= -4mA（TTL）	2.4	—	V
Low-level output voltage	V_{OL1}	V_{DD}=4.5V, I_{OL}= 100μA （CMOS）	—	V_{SS}+0.1	V
	V_{OL2}	V_{DD} =4.5V, I_{OL}= 4mA（TTL）	—	0.4	
High-level input voltage	V_{IH}	TTL	2.4	—	V
Low-level input voltage	V_{IL}	TTL	—	0.8	V

Supply current operating @20MHz	$I_{DD(OP)}$	TTL input (I_{OUT}=0) V_{IL}=0.2V, V_{IH}=5.5V, V_{DD}=5.5V, $\overline{PE}$ =5.5V, f=15.4MHz	—	100	mA
Supply current standby	$I_{DD(SB)}$	$V_{IL}=V_{SS}$+0.25V, $V_{IH}=V_{DD}$-0.25V, $\overline{CE}=V_{DD}$-0.25V, V_{DD} =5.5V	—	10	mA
Input leakage current	I_{IN}	V_I = 5.5V and 0V, T_A=25°C (all inputs except $\overline{PE}$)	-0.1	0.1	μA
		V_I= 5.5V, T_A=25°C ($\overline{PE}$)	—	1	μA
		V_I = 5.5V and 0V, T_A=-55°C and 125°C (all inputs except $\overline{PE}$)	-1	1	μA
		V_I= 5.5V, T_A=-55°C and 125°C ($\overline{PE}$)	—	1	μA
Three-state output leakage current	I_{OZ}	V_O = 0V~ V_{DD} , V_{DD} =5.5V $\overline{OE}$ =5.5V, T_A=25℃	-0.1	0.1	μA
		V_O = 0V~ V_{DD} , V_{DD} =5.5V $\overline{OE}$ =5.5V, T_A=125℃ and -55℃	-1	1	μA
Input capacitance	C_{IN}	f =1 MHz, T_A=25°C, open V_{DD}	—	15	pF
Bidirectional I/O capacitance	C_{IO}	f =1 MHz, T_A=25°C, open V_{DD}	—	15	pF

6.2 Read Cycle AC Electrical Characteristics (Pre and Post-Radiation)

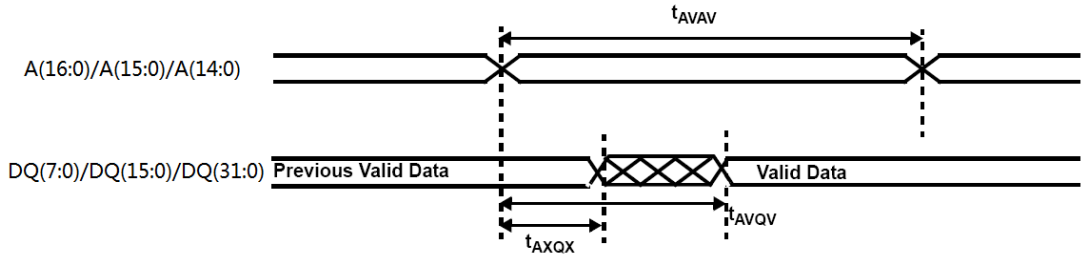
Table 5. Read Cycle AC Parameters

Parameter	**Symbol**	**Condition (4.5V≤ V_{DD} ≤ 5.5 V -55 °C ≤ T_A≤ 125 °C)**	**Limits**		**Unit**
			MIN	**MAX**	
Read cycle time1	t_{AVAV}	Figure 2	50	—	ns
Read access time23	t_{AVQV}		—	50	ns

Output hold time	t_{AXQX}		0		ns
$\overline{OE}$-controlled output 1enable time	t_{GLQX}	Figure 3	0	—	ns
$\overline{OE}$-controlled output enable time3	t_{GLQV}		—	15	ns
$\overline{OE}$-controlled output three-state time4	t_{GHQZ}		—	15	ns
$\overline{CE}$-controlled output enable time1	t_{ELQX}	Figure 4	0	—	ns
$\overline{CE}$-controlled access time3	t_{ELQV}		—	50	ns
$\overline{CE}$-controlled output three-state time4	t_{EHQZ}		—	15	ns

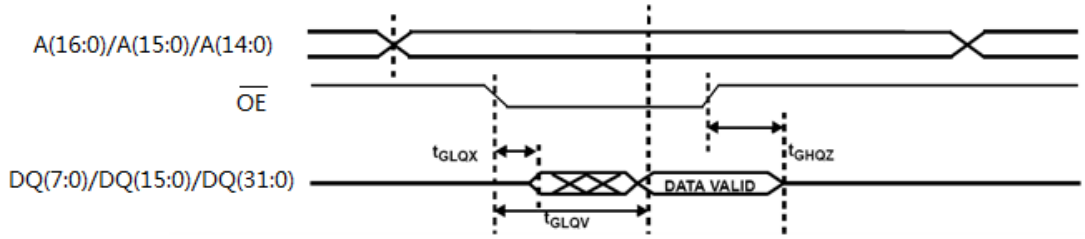
Notes:

1. t_{AVAV} is guaranteed by the test condition, t_{GLQX} and t_{ELQX} are design guaranteed but not tested.
2. The item is not tested for the blank device.
3. Measurement of data output occurs at the low to high or high to low transition mid-point.
4. Three-state is defined as a 500mV change from steady-state output voltage.



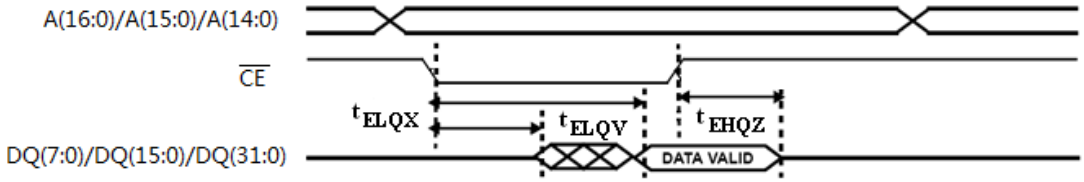
Assumptions: $\overline{CE}$ ≤V_{IL}(max), $\overline{OE}$≤V_{IL}(max), $\overline{PE}$≥V_{IH}(min); only one is higher than V_{IH}(min) among C08, C16 and C21, while the other two are lower than V_{IL}(max)

Figure 3 Read Cycle 1: Address Access



Assumptions: $\overline{CE}$ ≤V_{IL}(max), $\overline{PE}$≥V_{IH}(min) ; only one is higher than V_{IH}(min) among C08, C16 and C21, while the other two are lower than V_{IL}(max)

Figure 4 Read Cycle 2: Output Enable Controlled Access



Assumptions：$\overline{OE}$≤V_{IL}(max), $\overline{PE}$≥V_{IH}(min) ; only one is higher than V_{IH}(min) among C08, C16 and C21, while the other two are lower than V_{IL}(max)

Figure 5 Read Cycle 3: Chip Enable Controlled Access

7. Application

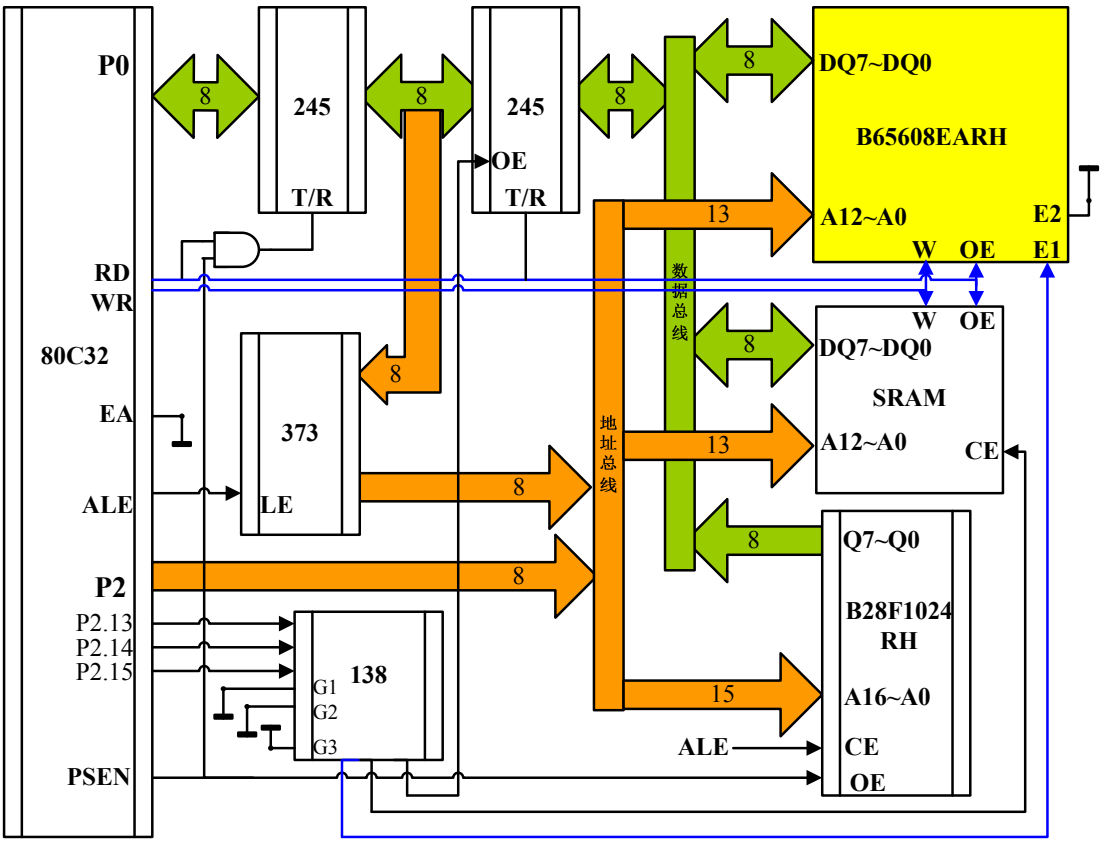


Figure 5 Typical application of B28F1024RH

8. Packaging

The PROM B28F1024RH utilizes QFP64 packaging as shown in Figure 6.

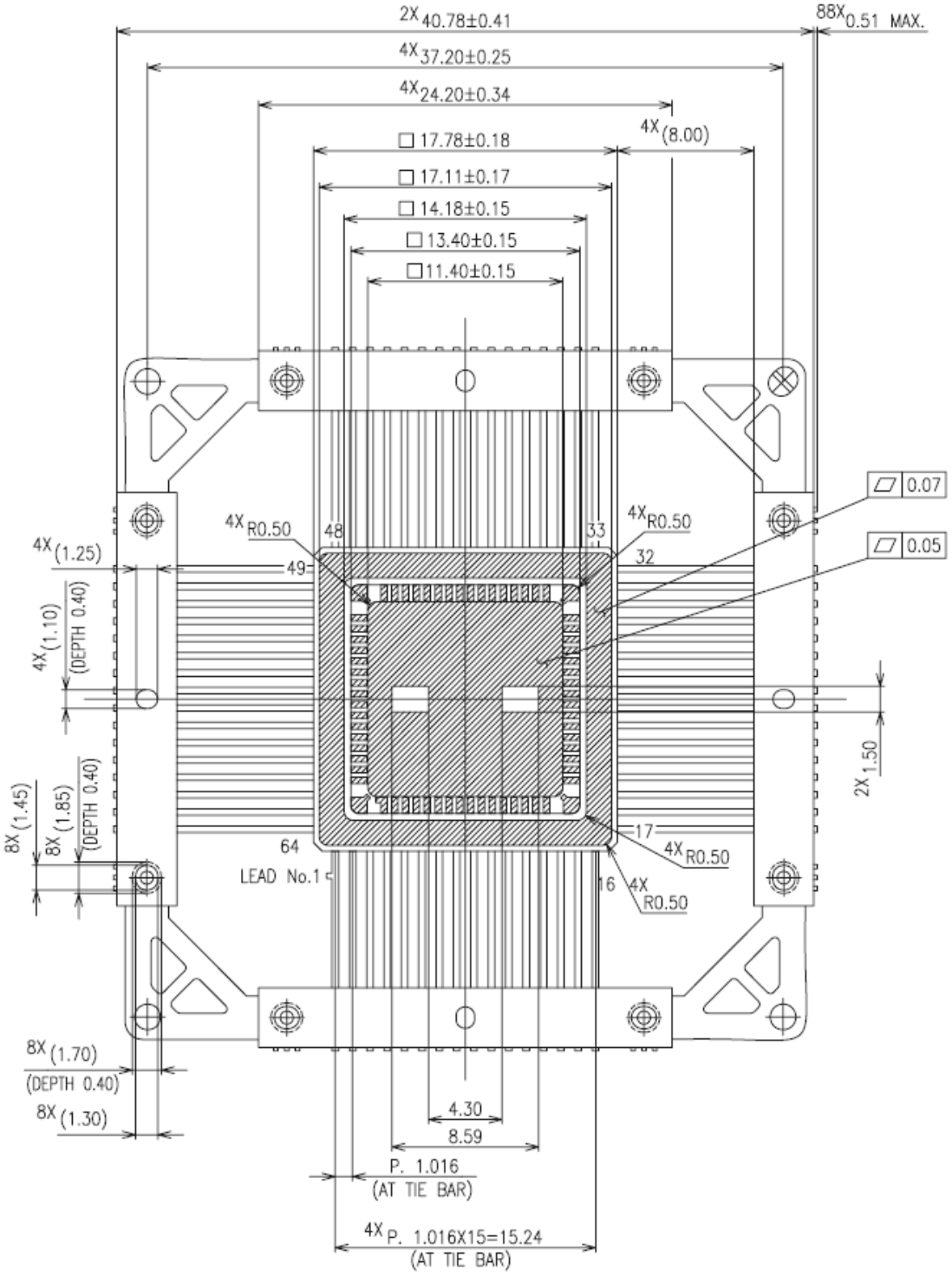


Figure 6 QFP64 Package Outline (unit: inch)

Appendix 1

Pin Descriptions are listed in Table 6:

Table 6. Pin Symbols and Functions

Pin No.	Symbol	I/O	Functions	Pin No.	Symbol	I/O	Functions
1	DQ[1]	I/O	bidirectional data	33	DQ[30]	O	Data Output
2	DQ[2]	I/O	bidirectional data	34	DQ[29]	O	Data Output
3	DQ[3]	I/O	bidirectional data	35	DQ[28]	O	Data Output
4	DQ[4]	I/O	bidirectional data	36	DQ[27]	O	Data Output
5	VDD		Power Supply	37	VDD		Power Supply
6	DQ[5]	I/O	bidirectional data	38	DQ[26]	O	Data Output
7	DQ[6]	I/O	bidirectional data	39	DQ[25]	O	Data Output
8	DQ[7]	I/O	bidirectional data	40	DQ[24]	O	Data Output
9	DQ[8]	O	Data Output	41	DQ[23]	O	Data Output
10	DQ[9]	O	Data Output	42	DQ[22]	O	Data Output
11	DQ[10]	O	Data Output	43	DQ[21]	O	Data Output
12	VSS		Ground	44	VSS		Ground
13	DQ[11]	O	Data Output	45	DQ[20]	O	Data Output
14	DQ[12]	O	Data Output	46	DQ[19]	O	Data Output
15	DQ[13]	O	Data Output	47	DQ[18]	O	Data Output
16	DQ[14]	O	Data Output	48	DQ[17]	O	Data Output
17	DQ[15]	O	Data Output	49	DQ[16]	O	Data Output
18	A[8]	I	Address Input	50	A[7]	I	Address Input
19	A[9]	I	Address Input	51	A[6]	I	Address Input
20	A[10]	I	Address Input	52	PE	I	Program Enable
21	VDD		Power Supply	53	VDD		Power Supply
22	A[11]	I	Address Input	54	A[5]	I	Address Input
23	A[12]	I	Address Input	55	A[4]	I	Address Input
24	A[13]	I	Address Input	56	A[3]	I	Address Input
25	A[14]	I	Address Input	57	A[2]	I	Address Input
26	A[15]	I	Address Input	58	A[1]	I	Address Input
27	A[16]	I	Address Input	59	A[0]	I	Address Input
28	VSS		Ground	60	VSS		Ground
29	VSS		Ground	61	C32	I	Bit width control

30	CE	I	Chip Enable	62	C16	I	Bit width control
31	OE	I	Output Enable	63	C08	I	Bit width control
32	DQ[31]	O	Data Output	64	DQ[0]	I/O	bidirectional data

Service & Supply

Address: No.2. Siyingmen N.Rd. Donggaodi Fengtai District,BeiJing,China
Department: Department of international cooperation
Telephone: +86(0)10-67968115-6751
Email：gjhz@mxtronics.com
Fax: +86(0)10-68757706
Zip code: 100076