Ver 1.3

Radiation-Hardened SRAM

Datasheet

Part Number：B8R512K39RH

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Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	09.20.2016		Document creation	
1.1	03.26.2017		Advance information datasheet document	
1.2	03.06.2018		Text modification	
1.3	27.07.2018		Template change	

TABLE OF CONTENTS

1. Features

- 20 ns maximum read time
- 10 ns minimum write time
- Asynchronous operation
- CMOS compatible inputs and output levels, three-state bidirectional data bus
- I/O Voltage 3.3 V，core Voltage 1.2 V
- ESD better than 2000 V
- Operational environment:
  - Total-dose: 100 K Rad (Si)
  - SEL Immune: > 75 MeV cm^2/mg
  - SEU Error Rate: ≤1E-10errors/bit-day in Geosynchronous Orbit
- Packaging options
  - 84-lead ceramic quad flatpack（CQFP84）

2. General Description

The B8R512K39RH is a high-performance radiation-hardened CMOS static SRAM organized as 512K words by 40 bits. Fabricated with industry-standard CMOS technology, the device works in asynchronous mode and requires no external clocks. The combination of radiation-hardness, fast access time, and low power consumption makes the B8R512K39RH ideal for high speed system designed for operation in radiation environments.

3. Block Diagram

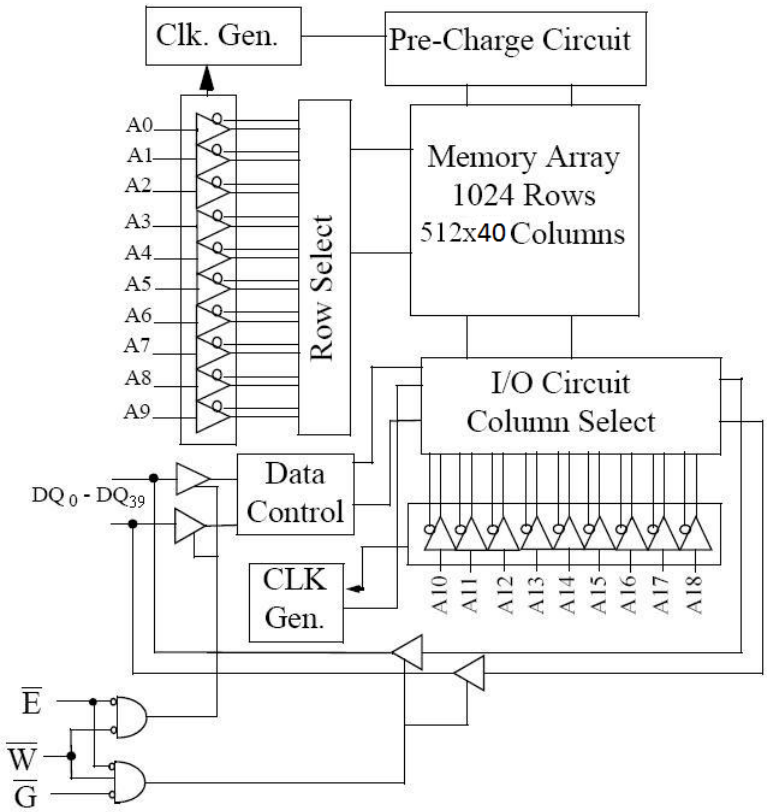


Figure 1. B8R512K39RH Block Diagram

4. Pin Description

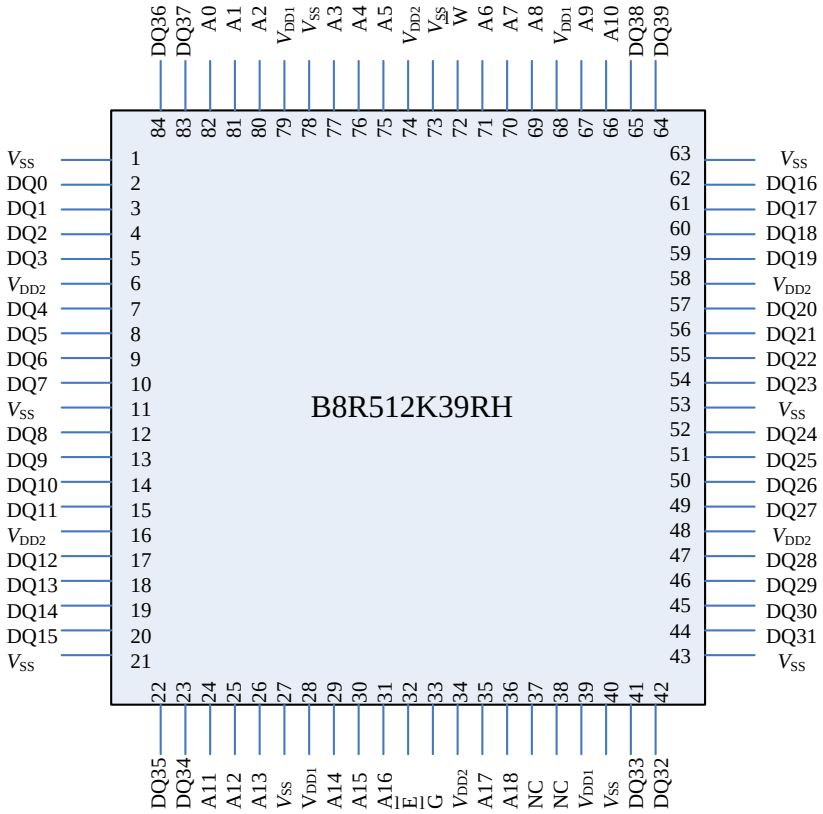


Figure 2. B8R512K39RH SRAM Pinout

Table 1. Pin Name

Pin Names	Functions
A0~A18	Address
DQ0~DQ39	Data Input / Output
$\overline{E}$	Chip Enable (Active Low)
$\overline{W}$	Write Enable (Low Write Enable, and High Read Enable)
$\overline{G}$	Output Enable (Active Low)
V_{DD1}	Power (1.2 V)
V_{DD2}	Power (3.3 V)
V_{SS}	Ground
NC	No Connect

5. Pin Configurations（Appendix 1）

6. Product Description

6.1 Quality Grade and Production Standard

The quality grade of the radiation-hardened SRAM B8R512K39RH is YB. And B8R512K39RH is up to GJB597A-1996 and the HX 64084A-2017 semiconductor IC standard.

6.2 Function Description

The B8R512K39RH has three control inputs, Chip Enable $\overline{E}$, Write Enable $\overline{W}$, and Output Enable ($\overline{G}$), 19 address inputs A (18:0), and 40 data lines, DQ0~DQ39.

Table 2. Device Operation Truth Table

Inputs			Outputs	
$\overline{G}$	$\overline{W}$	$\overline{E}$	I/O Mode	Mode
X[1]	X[1]	1	DQ(39:0) 3-State	Standby
X[1]	0	0	DQ(39:0) Data in	Write
0	1	0	DQ(39:0) Data out	Read
1	1	0	DQ(39:0) 3-State	Read DQ 3-State
Notes: 1. X = Don't care				

◆ **Read Cycle**

A combination of $\overline{W}$ greater than V_{IH}(min) and $\overline{E}$ less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 4, is initiated by a change in address inputs while the chip is in read state ($\overline{E}$=0, $\overline{G}$=0，$\overline{W}$=1). Valid data appears on data outputs DQ(39:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 5, is initiated by a negative pulse of $\overline{E}$, while $\overline{G}$=0，$\overline{W}$=1, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the word addressed by A(18:0) is accessed and appears at the data outputs DQ(39:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 6, is initiated by a negative pulse of $\overline{G}$,while $\overline{E}$=0, $\overline{W}$=1, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

◆ **Write Cycle**

A combination of $\overline{W}$ and $\overline{E}$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 7, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E}$=0. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E}$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the pins DQ(39:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 8, is defined by a write terminated by $\overline{E}$ going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by $\overline{E}$ going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the pins DQ(39:0) to avoid bus contention.

6.3 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Limits
V_{DD1}	Core supply voltage	-0.3V ~ +1.35 V
V_{DD2}	I/O supply voltage	-0.3V ~ +3.8 V
$V_{I/O}$	Voltage on any pin	-0.3V ~ +3.8 V

T_{STG}	Storage Temperature	-65℃ ~ 150℃
P_D	Maximum power dissipation	2W
T_J	Maximum junction temperature	+150℃
$R_{th(J-C)}$	Thermal resistance, junction-to-case	5℃/W

6.4 Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD1}	Core supply voltage	1.08 V ~ 1.32V
V_{DD2}	I/O supply voltage	2.97 V ~ 3.63 V
T_C	Case temperature range	-55℃ ~ +125℃
V_I	DC input voltage	0 V ~ V_{DD2}
Notes: The correct power-up sequence should be V_{DD1}--> V_{DD2}.		

7. Electrical Characteristics

7.1 DC Electrical Characteristics

Table 5. DC Parameter Table (Ⅰ)

Parameter	Symbol	Condition (GND=0V，-55℃≤T_A≤125℃) 1.08V≤V_{DD1}≤1.32V， 2.97V≤V_{DD2}≤3.63V)	Limits		UNIT
			MIN	MAX	
High-level input voltage	V_{IH}		0.7*V_{DD2}	—	V
Low-level input voltage	V_{IL}		—	0.3*V_{DD2}	V
High-level output voltage	V_{OH}	V_{DD2}= V_{DD2}(min), I_{OH}= -4mA	0.8*V_{DD2}	—	V
Low-level output voltage	V_{OL}	V_{DD2}= V_{DD2}(min), I_{OL}= 8mA	—	0.2*V_{DD2}	V

input leakage current	I_{IN}	$V_{IN}=V_{DD2}/V_{SS}$ all inputs are tested		-2	2	μA
Three-state output leakage current	I_{OZ}	$V_O=V_{DD2}/V_{SS}$, $V_{DD2}=V_{DD2}$(max)， $\overline{G}=V_{DD2}$(max)		-2	2	μA
Operation current @1MHz	$I_{DD1(OP1)}$	CMOS input ： $V_{IL}=V_{SS}$+0.2V, $V_{IH}=V_{DD2}$-0.2V, I_{OUT}=0 $V_{DD1}=V_{DD1}$(max)， $V_{DD2}=V_{DD2}$(max)	V_{DD1}=1.32V	—	50	mA
			V_{DD1}=1.2V	—	50	mA
Operation current @50MHz	$I_{DD1(OP2)}$	CMOS input ： $V_{IL}=V_{SS}$+0.2V, $V_{IH}=V_{DD2}$-0.2V, I_{OUT}=0， $V_{DD1}=V_{DD1}$(max)， $V_{DD2}=V_{DD2}$(max)	V_{DD1}=1.32V	—	70	mA
			V_{DD1}=1.2V	—	60	mA
Operation current @1MHz	$I_{DD2(OP1)}$	CMOS input ： $V_{IL}=V_{SS}$+0.2V $V_{IH}=V_{DD2}$-0.2V, I_{OUT}=0， $V_{DD2}=V_{DD2}$(max) ,$V_{DD1}=V_{DD1}$(max)		—	5	mA
Operation current @50MHz	$I_{DD2(OP2)}$	CMOS input ： $V_{IL}=V_{SS}$+0.2V $V_{IH}=V_{DD2}$-0.2V， I_{OUT}=0 $V_{DD2}=V_{DD2}$(max) ,$V_{DD1}=V_{DD1}$(max)		—	5	mA
Standby current @0Hz	$I_{DD1(SB)}$	CMOS input , I_{OUT}=0 $\overline{E}=V_{DD2}$-0.2V $V_{DD2}=V_{DD2}$(max)， $V_{DD1}=V_{DD1}$(max)		—	50	mA
Standby current @0Hz	$I_{DD2(SB)}$	CMOS input , I_{OUT}=0 $\overline{E}=V_{DD2}$-0.2V $V_{DD2}=V_{DD2}$(max)， $V_{DD1}=V_{DD1}$(max)		—	3	mA
Standby current A<18:0>@50MHz	$I_{DD1(SB)}$	CMOS input , I_{OUT}=0 $\overline{E}=V_{DD2}$-0.2V $V_{DD2}=V_{DD2}$(max)， $V_{DD1}=V_{DD1}$(max)		—	50	mA
Standby current A<18:0>@50MHz	$I_{DD2(SB)}$	CMOS input , I_{OUT}=0 $\overline{E}=V_{DD2}$-0.2V $V_{DD2}=V_{DD2}$(max)， $V_{DD1}=V_{DD1}$(max)		—	3	mA
Note：* the post-irradiation performance is guaranteed at 25℃						

7.2 Read Cycle AC Electrical Characteristics

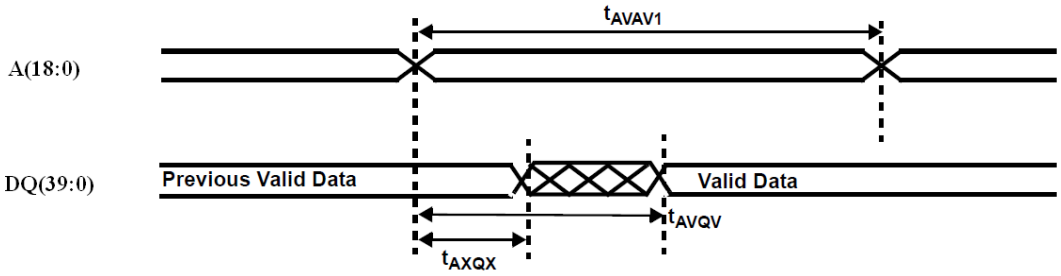
Table 6. Read Cycle AC Parameters

Parameter	**Symbol**	**Condition** (V_{DD1}=V_{DD1}(min), V_{DD2}=V_{DD2}(min), -55℃≤ T_A≤ 125℃)	**Limits**		**UNIT**
			MIN	**MAX**	
Read cycle time	t_{AVAV}[1]	Figure 4	20	—	ns
Address to data valid	t_{AVQV}		—	20	ns
Output hold time from address change	t_{AXQX}[1]		3	—	ns
$\overline{G}$-controlled output enable time	t_{GLQX}[1]	Figure 6	2	—	ns
$\overline{G}$-controlled output data valid	t_{GLQV}		—	10	ns
$\overline{G}$-controlled output three-state time	t_{GHQZ}[1,2]		2	8	ns
$\overline{E}$ -controlled output enable time	t_{ETQX}[1]	Figure 5	5	—	ns
$\overline{E}$ -controlled access time	t_{ETQV}		—	20	ns
$\overline{E}$ -controlled output three-state time	t_{EFQZ}[1,2]		2	9	ns

Notes:

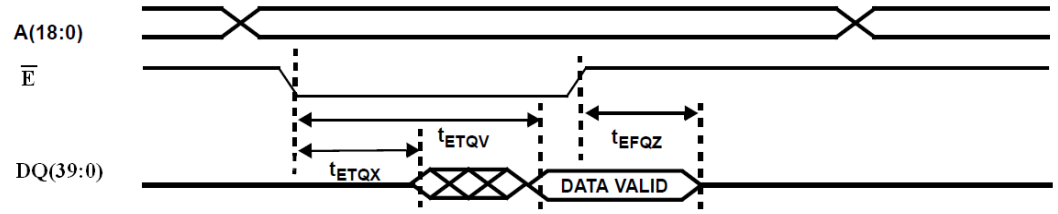
* the post-irradiation performance is guaranteed at 25℃

1. Guaranteed but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.



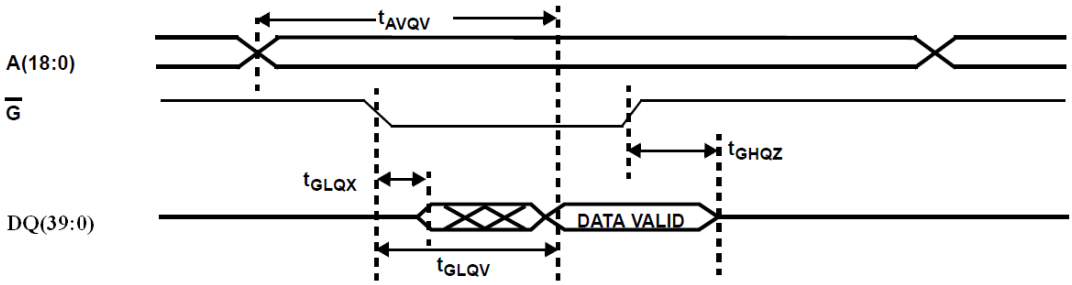
Assumptions： $\overline{E}$ ≤V_{IL}(max), $\overline{G}$≤V_{IL}(max), $\overline{W}$≥V_{IH}(min)

Figure 4. SRAM Read Cycle 1: Address Access



Assumptions： $\overline{G}$≤V_{IL}(max), $\overline{W}$≥V_{IH}(min)

Figure 5. SRAM Read Cycle 2: Chip Enable Access



Assumptions: $\overline{E}$ ≤V_{IL}(max), $\overline{W}$≥V_{IH}(min)

Figure 6. SRAM Read Cycle 3: Output Enable Access

7.3 Write Cycle AC Electrical Characteristics

Table 7. Write Cycle AC Parameter (Ⅰ)

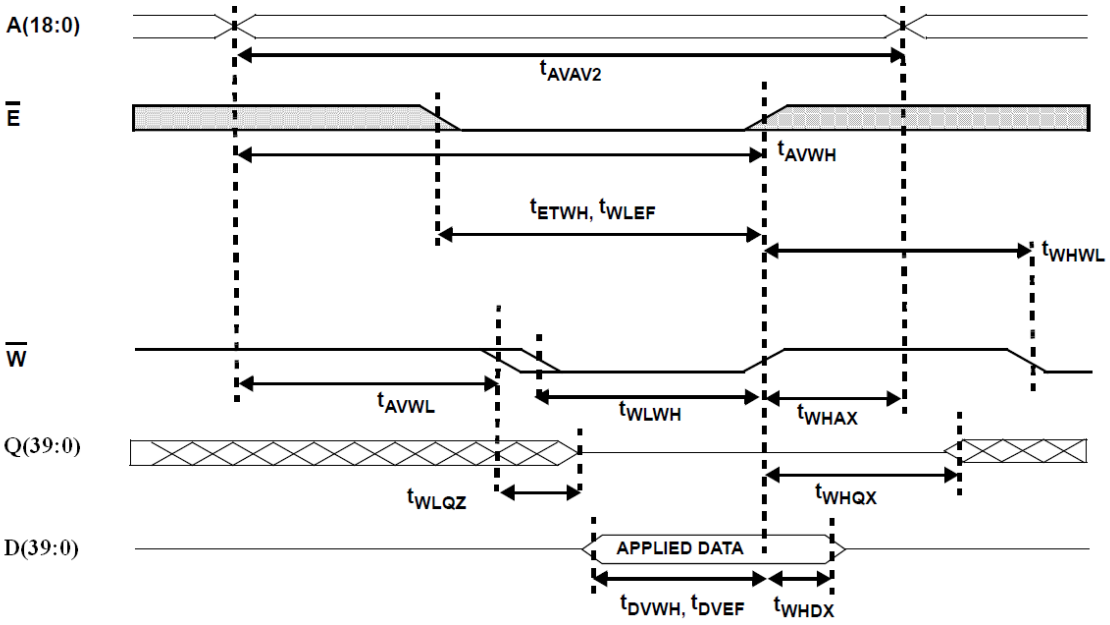
Parameter	Symbol	Condition (V_{DD1}=V_{DD1}(min), V_{DD2}=V_{DD2}(min), -55℃≤T_A≤125℃)	Limits		UNIT
			MIN	MAX	
Write cycle time	t_{AVAV}[1]	Figure 7 & Figure 8	10	—	ns
Chip enable to end of write	t_{ETWH}[1]	Figure 7	6	—	ns
Address setup time for write ($\overline{E}$-controlled)	t_{AVET}[1]		0	—	ns
Address setup time for write ($\overline{W}$-controlled)	t_{AVWL}[1]	Figure 7	0	—	ns
Write pulse width	t_{WLWH}[1]	Figure 7	6	—	ns
Address hold time for write ($\overline{W}$-controlled)	t_{WHAX}[1]	Figure 7	2	—	ns
Address hold time for chip enable ($\overline{E}$-controlled)	t_{EFAX}[1]	Figure 8	2	—	ns
$\overline{W}$-controlled three-state time	t_{WLQZ}[2,3]	Figure 7	—	9	ns
$\overline{W}$-controlled output enable time	t_{WHQX}[2]	Figure 7	2	—	ns
Chip enable pulse width ($\overline{E}$-controlled)	t_{ETEF}[1]	Figure 8	6	—	ns
Data setup time	t_{DVWH}[1]	Figure 7	2	—	ns
Data hold time	t_{WHDX}[1]	Figure 7	2	—	ns
Chip enable controlled write pulse width	t_{WLEF}[1]	Figure 8	6	—	ns
Data setup time	t_{DVEF}[1]	Figure 8	2	—	ns
Data hold time	t_{EFDX}[1]	Figure 8	2	—	ns

Address valid to end of write	t_{AVWH}[1]	Figure 7	6	—	ns
Write disable time	t_{WHWL}[1]	Figure 7	2	—	ns

Notes:

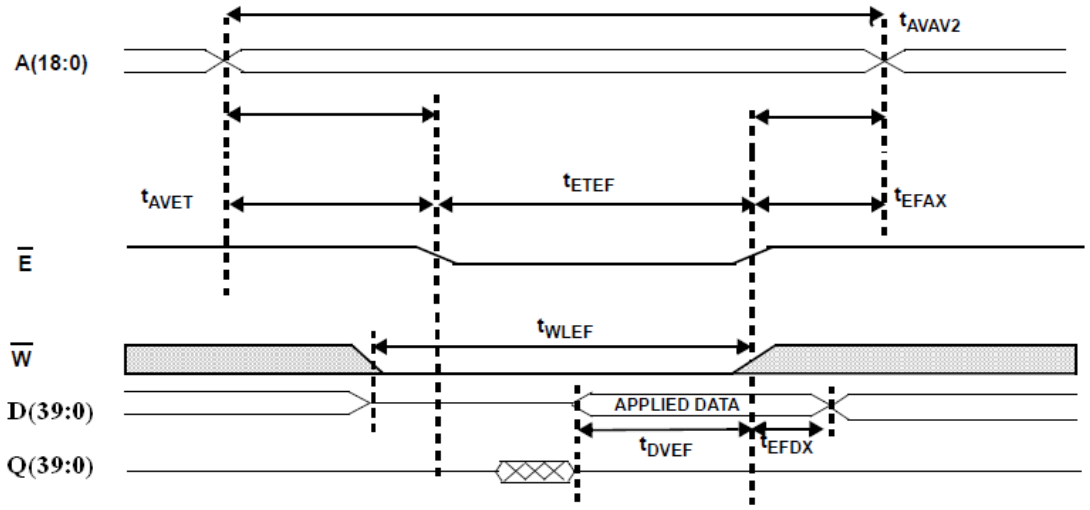
* the post-irradiation performance is guaranteed at 25℃

1. Guaranteed by test vectors
2. Guaranteed but not tested
3. Three-state is defined as 200mV change from steady-state output voltage.
4. the parameters are Tested with $\overline{G}$ high.



Assumptions: $\overline{G} \leq V_{IL}$(max)

Figure 7. SRAM Write Cycle 1: $\overline{W}$-controlled Access



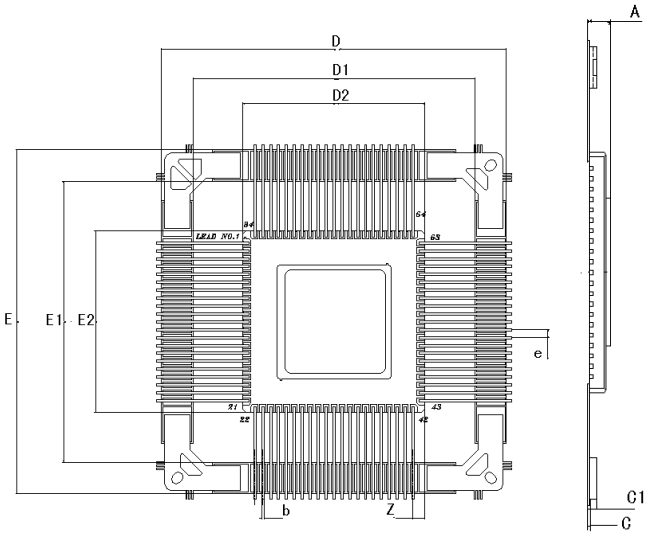
Assumption: $\overline{G} \leq V_{IL}(max)$

Figure 8. SRAM Write Cycle 2: Enable-chip Controlled Access

8. Typical Application（Appendix 2）

9. Packaging

The SRAM B8R512K39RH utilizes 84-Lead Ceramic Quad Flatpack as shown in Figure 9 and the corresponding dimensions are listed in Table 8, which is accordance with GB/T7092.



Notes:

1. The lid is electrically connected to VSS.

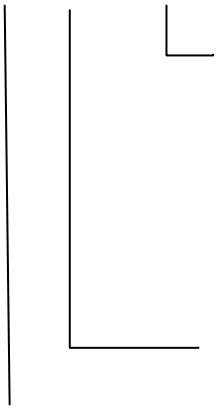
Figure 9. Package Outline

Table 8. Package Dimensions

Symbol	Min	Normal	Max
A	1.30	—	2.90
b	0.23	—	0.53
C	0.10	—	0.20
C1	0.5	—	1.28
D/E	54.07	—	56.67
D1/E1	44.22	—	46.90
D2/E2	28.62	—	29.80
e	—	1.27	—
Z	1.19	—	2.63

10. Naming Rule

B8R512K39RH



Design Type:
Radiation-Hardened

Device Type:
(8R512K39)=512K x 39 SRAM

Company code

Appendix 1

Pin Descriptions are listed in Table 9：

Table 9. Pin Symbols and Functions

Pin NO.	Functions	Functions	Pin NO.	Symbol	Functions
1	V_{SS}	Ground	43	V_{SS}	Ground
2	DQ0	I/O	44	DQ31	I/O
3	DQ1	I/O	45	DQ30	I/O
4	DQ2	I/O	46	DQ29	I/O
5	DQ3	I/O	47	DQ28	I/O
6	V_{DD2}	Power(3.3V)	48	V_{DD2}	Power(3.3V)
7	DQ4	I/O	49	DQ27	I/O
8	DQ5	I/O	50	DQ26	I/O
9	DQ6	I/O	51	DQ25	I/O
10	DQ7	I/O	52	DQ24	I/O
11	V_{SS}	Ground	53	V_{SS}	Ground
12	DQ8	I/O	54	DQ23	I/O
13	DQ9	I/O	55	DQ22	I/O
14	DQ10	I/O	56	DQ21	I/O
15	DQ11	I/O	57	DQ20	I/O
16	V_{DD2}	Power(3.3V)	58	V_{DD2}	Power(3.3V)
17	DQ12	I/O	59	DQ19	I/O
18	DQ13	I/O	60	DQ18	I/O
19	DQ14	I/O	61	DQ17	I/O
20	DQ15	I/O	62	DQ16	I/O
21	V_{SS}	Ground	63	V_{SS}	Ground
22	DQ35	I/O	64	DQ39	I/O
23	DQ34	I/O	65	DQ38	I/O
24	A11	Address	66	A10	Address
25	A12	Address	67	A9	Address
26	A13	Address	68	V_{DD1}	Power(1.2V)

27	V_{SS}	Ground	69	A8	Address
28	V_{DD1}	Power(1.2V)	70	A7	Address
29	A14	Address	71	A6	Address
30	A15	Address	72	$\overline{W}$	Read and Write Enable
31	A16	Address	73	V_{SS}	Ground
32	$\overline{E}$	Chip Enable	74	V_{DD2}	Power(3.3V)
33	$\overline{G}$	Output Enable	75	A5	Address
34	V_{DD2}	Power(3.3V)	76	A4	Address
35	A17	Address	77	A3	Address
36	A18	Address	78	V_{SS}	Ground
37	NC	No connect	79	V_{DD1}	Power(1.2V)
38	NC	No connect	80	A2	Address
39	V_{DD1}	Power(1.2V)	81	A1	Address
40	V_{SS}	Ground	82	A0	Address
41	DQ33	I/O	83	DQ37	I/O
42	DQ32	I/O	84	DQ36	I/O

Appendix 2

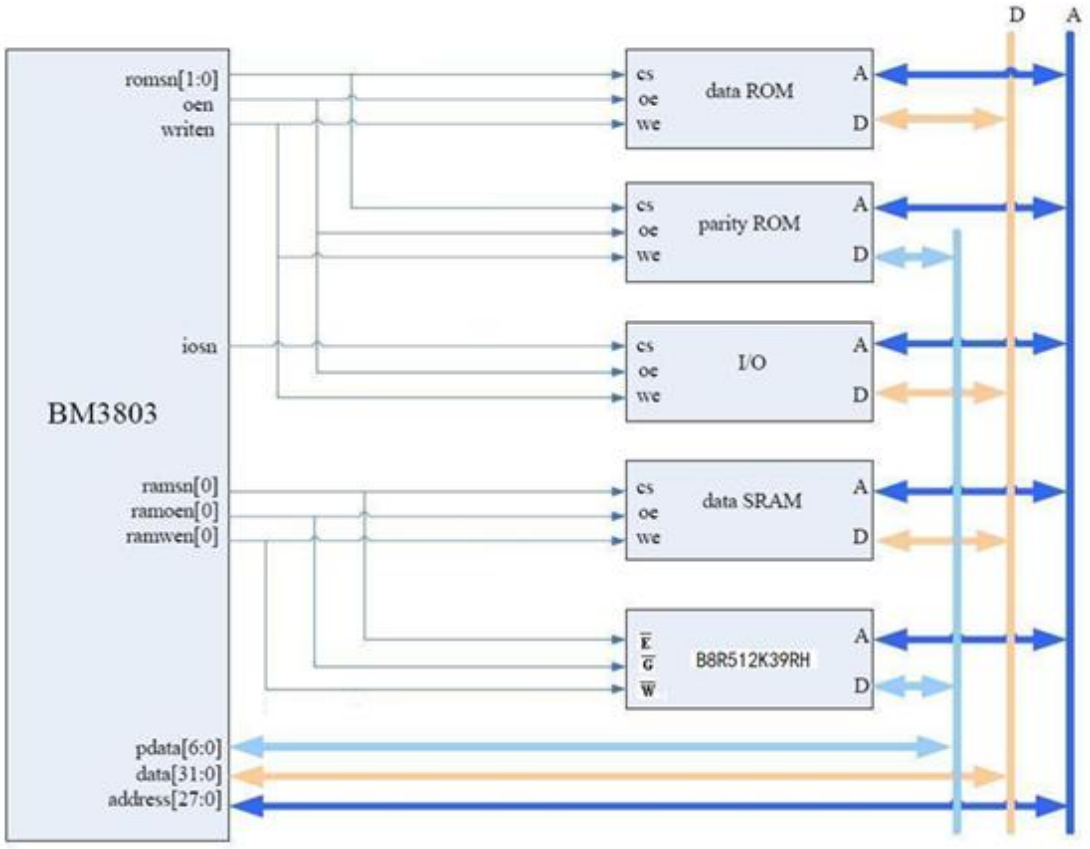


Figure 10. Typical Application

Figure 10 illustrates a typical application system, which consists of a CPU and an SRAM (B8R512K39RH) chip. The B8R512K39RH serves as data storage for the CPU, while the CPU controls the SRAM operation properly.

For starting up normally, both 3.3 and 1.2 V power supply should be applied to the SRAM correctly, then it will operate according to the control signals sent by the CPU. Normally the CPU will write some data into the SRAM in the first place. For this operation, $\overline{W}$ and $\overline{E}$ should be set lower than V_{IH} (max), and either of two different write cycles described in Section 7.3 can be used to realize the writing, as long as the signals generated by the CPU satisfy the relevant timing sequence requirements.

The read operation can be implemented similarly. For this operation, $\overline{W}$ should be set higner than V_{IH} (min) and $\overline{E}$ should be set lower than V_{IH} (max). The B8R512K39RH offers three different kinds of read cycles, the selection of which can be decided according to the demand of whole system. Also, proper signal sequence is required for successful read operation.

Notes:

1. Supply voltage sequencing is recommended to be V_{DD2} prior to V_{DD1}.
2. Supply voltage is required to be as stable as possible.
3. The input should not be suspend in midair. The transition of the input signal should be less than 10ns ,voltage from Vil to Vih.
4. The output should not be connected to supply voltage or V_{SS}.

The lid is electrically connected to V_{SS}.

Service & Supply

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