Ver 1.2

Radiation-Hardened SRAM

Datasheet

Part Number：B28F256LVRH

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Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	11.20.2015		Document creation	
1.1	09.25.2016	7	Advance Packaging information	
1.2	03.06.2018		Text and wording modifications	

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1. Features

- Asynchronous operation, functionally compatible with Aeroflex UT28F256LVQLE PROM
- 65 ns maximum access time (-55 ℃ ~ 125 ℃)
- CMOS compatible inputs and outputs levels, three-state bidirectional data bus
- Voltage supply: 3.0V ~ 3.6V
- $I_{OP@15.4MHz}$|max=50mA
- ESD better than 2000 V
- Operational environment:
  Total-dose: 100 K Rad (Si)
  SEL Immune: > 75 MeV cm^2/mg
  SEU: > 37 MeV cm^2/mg
- Packaging options:
  28-lead ceramic DIP (CDIP28)
  28-lead FP

2. General Description

The B28F256LVRH PROM is a high performance, asynchronous, radiation-hardened, 32K x 8 programmable memory device. The B28F256LVRH PROM features fully asynchronous operation requiring no external clocks or timing strobes and is functionally compatible with Aeroflex UT28F256LVQLE. B28F256LVRH needs to be programmed by the special programmer. The combination of radiation-hardness, fast access time, and low power consumption make the B28F256LVRH ideal for high speed systems designed for operation in radiation environments.

3. Pin Description

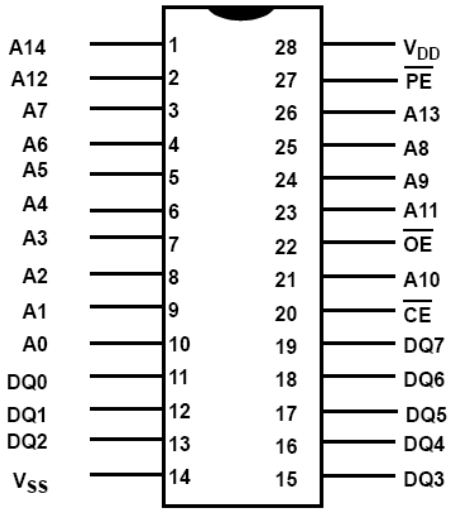


Figure 1 B28F256LVRH PROM Pin Figuration8)

Table 1. Pin Names

Pin Names	Functions
A0~A14	Address
DQ0~DQ7	Data Input / Output
$\overline{CE}$	Chip Enable (Active Low)
$\overline{PE}$	Program Enable (Active Low)
$\overline{OE}$	Output Enable (Active Low)
V_{DD}	Power (3.3 V)
V_{SS}	Ground

4. Pin Configurations（Appendix 1）

5. Product Description

5.1 Function Description

The B28F256LVRH has three control inputs: Chip Enable ($\overline{CE}$), Program Enable ($\overline{PE}$), and Output Enable ($\overline{OE}$); fifteen address inputs, A(14:0); and eight bidirectional data lines, DQ(7:0). $\overline{CE}$ is the device enable input that controls chip selection, active, and standby modes. Asserting $\overline{CE}$ causes the decode of the fifteen address inputs and one of 32,768 words in the memory is selected. $\overline{PE}$ controls program and read operations. During a read cycle, $\overline{OE}$ must be asserted to enable the outputs.

Table 2. Device Operation Truth Table

Inputs			Outputs	
$\overline{OE}$	$\overline{PE}$	$\overline{CE}$	I/O Mode	Mode
X[1]	1	1	DQ(7:0) 3-State	Standby
0	1	0	DQ(7:0) Data out	Read
1	0	0	DQ(7:0) Data in	Write
1	1	0	DQ(7:0) 3-State	Read

Notes: The other combinations of $\overline{CE}$, $\overline{PE}$, and $\overline{OE}$, which are not listed in the table are not allowed.

1. X = Don't care

◆ **Read Cycle**

A combination of $\overline{PE}$ greater than V_{IH}(min) and $\overline{CE}$ less than V_{IL}(max) defines a read cycle, after programmed the $\overline{PE}$ pin is strongly recommend to connected with the VDD pin. When $\overline{OE}$ is asserted, the data can be get from DQ(7:0). Read access

time is measured from the latter of chip enable, output enable, or valid address to valid data output.

Read Cycle 1, the Address Access in Figure 2, is initiated by a change in address inputs while the chip is enabled with $\overline{OE}$ asserted and $\overline{PE}$ deasserted. Valid data appears on data outputs DQ (7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

Read Cycle 2, the Chip Enable-controlled Access in Figure 3, is initiated by $\overline{CE}$ going active while $\overline{OE}$ remains asserted, $\overline{PE}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 8-bit word addressed by A (14:0) is accessed and appears at the data outputs DQ (7:0).

Read Cycle 3, the Output Enable-controlled Access in Figure 4, is initiated by $\overline{OE}$ going active while $\overline{CE}$ is asserted, $\overline{PE}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ELQV} have not been satisfied.

5.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD}	Positive supply voltage	3.0 V ~ 3.6 V
T_C	Case temperature range	-55℃ ~ +125℃
V_I	DC input voltage	0 V ~ V_{DD}

6. Electrical Characteristics

6.1 DC Electrical Characteristics

Table 4. DC Parameter Table

Parameter	Symbol	Condition -55℃≤T≤125℃; 3V≤V_{DD}≤3.6V	Limits		UNIT
			MIN	MAX	
High-level output voltage	V_{OH1}	V_{DD}=3V, I_{OH}= -100uA	V_{DD}-0.15	—	V
	V_{OH2}	V_{DD}=3V, I_{OH}= -1mA	V_{DD}-0.3	—	
Low-level output	V_{OL1}	V_{DD}=3.0V, I_{OL}= 100uA	—	V_{SS}+0.05	V

voltage	V_{OL2}	V_{DD}=3V, I_{OH}= 1mA	—	V_{SS}+0.10	
High-level input voltage	V_{IH}	—	0.7×V_{DD}	—	V
Low-level input voltage	V_{IL}	—	—	0.3×V_{DD}	V
Three-state output leakage current	I_{OZ}	V_O = 0V~ V_{DD} ， V_{DD} =3.6V $\overline{OE}$ =3.6V， T_A=25℃	-0.1	0.1	μA
		V_O = 0V~ V_{DD} ， V_{DD} =3.6V $\overline{OE}$ =3.6V， T_A=125℃ and -55℃	-1	1	μA
Input leakage current	I_{IN}	V_I = 5.5V and 0V, T_A=25 ℃ (all inputs except $\overline{PE}$)	-0.1	0.1	μA
		V_I= 5.5V， T_A=25 ℃ ($\overline{PE}$)	—	1	μA
		V_I = 5.5V and 0V, T_A=-55 ℃ and 125 ℃(all inputs except $\overline{PE}$)	-1	1	μA
		V_I= 5.5V， T_A=-55 ℃ and 125 ℃ ($\overline{PE}$)	—	1	μA
Supply current standby	$I_{DD(SB)}$	I_{OUT}=0, V_{IL}=V_{SS}+0.25V ， V_{IH}= V_{DD}-0.25V ， $\overline{CE}$ =V_{DD}-0.25V ， V_{DD} =3.6V	—	10	mA
Supply current operating @15.4MHz	$I_{DD(OP)}$	I_{OUT}=0,V_{IL}=0.2V， V_{IH}=3.0V， V_{DD} =3.6V， $\overline{PE}$=3.6V， f=15.4MHz	—	50	mA

6.2 Read Cycle AC Electrical Characteristics

Table 5. Read Cycle AC Parameters

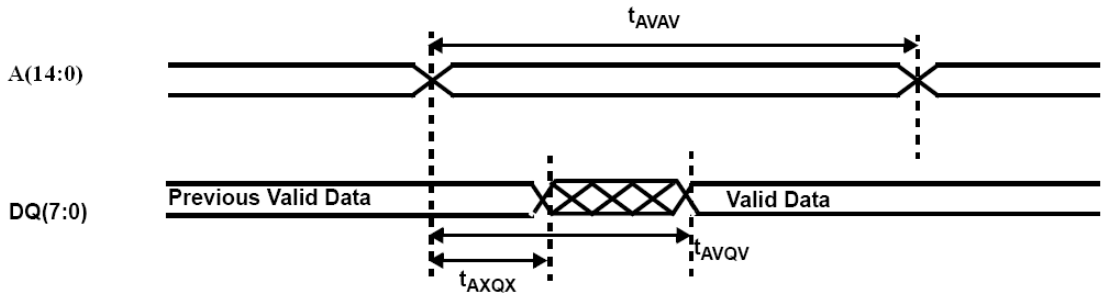
Parameter	**Symbol**	**Condition (3.0V≤ V_{DD} ≤ 3.6 V -55 ℃ ≤ T_A≤ 125 ℃)**	**Limits**		**Unit**
			MIN	**MAX**	
Read cycle time1	t_{AVAV}	Figure 2	65	—	ns
Read access time23	t_{AVQV}		—	65	ns
Output hold time	t_{AXQX}		0		ns
$\overline{CE}$-controlled output enable time1	t_{ELQX}	Figure 3	0	—	ns

$\overline{CE}$-controlled access time3	t_{ELQV}		—	65	ns
$\overline{CE}$-controlled output three-state time4	t_{EHQZ}		—	35	ns
$\overline{OE}$-controlled output 1enable time	t_{GLQX}	Figure 4	0	—	ns
$\overline{OE}$-controlled output enable time3	t_{GLQV}		—	35	ns
$\overline{OE}$-controlled output three-state time4	t_{GHQZ}		—	35	ns

Notes:

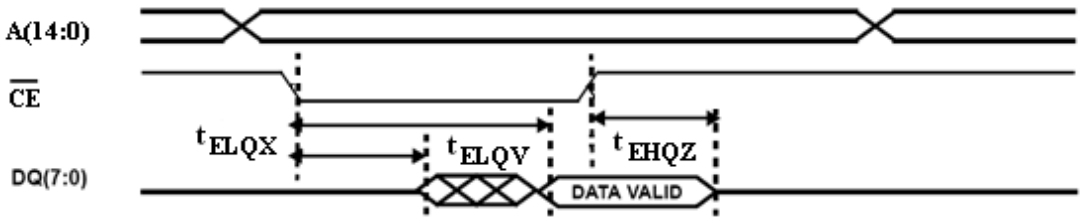
*Post-radiation performance guaranteed at 25℃ per MIL-STD-883 Method 1019.

1. t_{AVAV} is guaranteed by the test condition, t_{GLQX} and t_{ELQX} are design guaranteed but not tested.
2. The item is not tested for the blank device.
3. Measurement of data output occurs at the low to high or high to low transition mid-point.
4. Three-state is defined as a 200mV change from steady-state output voltage.



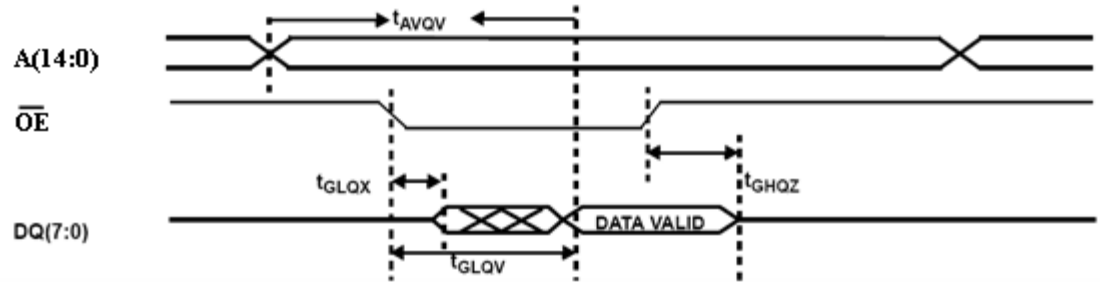
Assumptions: $\overline{CE} \leq V_{IL}(max)$, $\overline{OE} \leq V_{IL}(max)$, $\overline{PE} \geq V_{IH}(min)$, the $\overline{PE}$ pin is strongly recommend to connected with the VDD pin

Figure 2. Read Cycle 1: Address Access



Assumptions：$\overline{OE}$≤V_{IL}(max), $\overline{PE}$≥V_{IH}(min) , the $\overline{PE}$ pin is strongly recommend to connected with the VDD pin

Figure 3. Read Cycle 2: Chip Enable Access

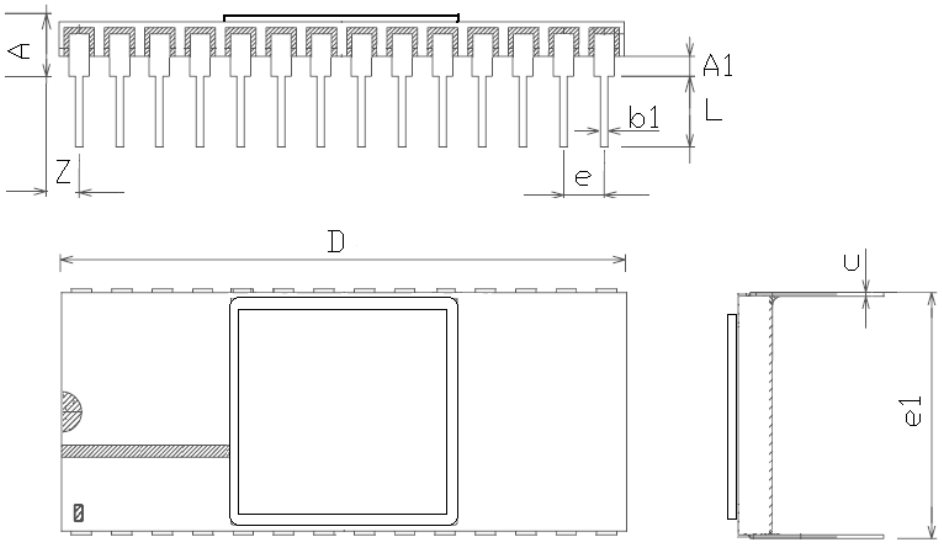


Assumptions: $\overline{CE}$ ≤V_{IL}(max), $\overline{PE}$≥V_{IH}(min) , the $\overline{PE}$ pin is strongly recommend to connected with the VDD pin

Figure 4. Read Cycle 3: Output Enable Access

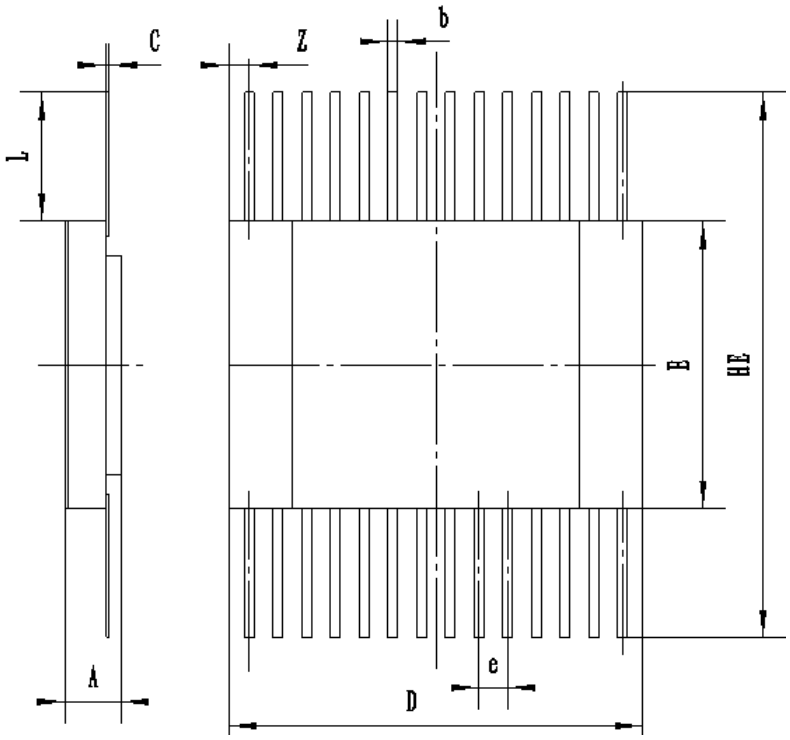
7. Packaging

The PROM B28F256LVRH utilizes 28-Lead DIP as shown in Figure 5 and 28-Lead flatpack as shown in Figure 6.



Symbols	Size (Unit: mm)		
	Min	BSC	Min
A	2.83	——	4.03
A1	0.72	——	1.82
b1	0.20	——	0.70
c	0.10	——	0.40
e	2.11	——	2.97
e1	14.93	——	16.04
D	34.90	——	36.22
Z	0.59	——	1.95
L	2.54	——	4.74

Figure 6. DIP28 Package Outline



Symbols	Size (Unit: mm)		
	Min	BSC	Max
A	2.30	——	2.90
b	0.35	——	0.55
c	0.08	——	0.18
e	0.89	——	1.65
Z	0.65	——	1.15
D	17.59	——	18.79
E	12.20	——	13.20
HE	22.70	——	33.45
L	6.00	——	10.83

Figure 7. FP28 Package Outline

Appendix 1

Pin Descriptions are listed in Table 6:

Table 6. Pin Symbols and Functions

Pin No.	Symbol	Functions	Pin No.	Symbol	Functions
1	A14	Address Input	15	Q3	bidirectional data
2	A12	Address Input	16	Q4	Bidirectional data
3	A7	Address Input	17	Q5	Bidirectional data
4	A6	Address Input	18	Q6	bidirectional data
5	A5	Address Input	19	Q7	Bidirectional data
6	A4	Address Input	20	CE	Chip Enable
7	A3	Address Input	21	A10	Address Input
8	A2	Address Input	22	OE	Output Enable
9	A1	Address Input	23	A11	Address Input
10	A0	Address Input	24	A9	Address Input
11	DQ0	bidirectional data	25	A8	Address Input
12	DQ1	Bidirectional data	26	A13	Address Input
13	DQ2	Bidirectional data	27	PE	Program Enable
14	V_{SS}	Ground	28	V_{DD}	3.3V Power Supply

Service & Supply

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