Ver 1.1

Radiation-Hardened LVDS QUAD RECEIVER

Datasheet

Part Number：B54LVDS032LVRH

北京微电子技术研究所

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	20170324	——	——	
1.1	20180313	——	change version	

TABLE OF CONTENTS

1. Features

- >400.0 Mbps (200 MHz) switching rates
- +340mV differential signaling
- 3.3 V power supply
- TTL compatible outputs
- Cold spare on all pins
- Ultra low power CMOS technology
- 4ns maximum propagation delay
- 350ps maximum differential skew
- Radiation-hardened design:
  - Total-dose: 300 krad(Si)
  - Latchup immune (LET >75MeV-cm^2/mg)
- Packaging options:
  - 16-lead flatpack (dual in-line)
- Compatible with IEEE 1596.3 SCI LVDS s:
- Compatible with ANSI/TIA/EIA 644-1996 LVDS Standard

2. General Description

The B54LVDS032LVRH Quad Receiver is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400.0 Mbps (200MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The B54LVDS032LVRH accepts low voltage (340mV) differential input signals and translates them to 3V CMOS output levels. The receiver supports a three-state function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100 Ω) input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

The B54LVDS032LVRH and companion quad line driver B54LVDS031LVRH provides new alternatives to high power pseudo-ECL devices.

All pins have Cold Spare buffers. These buffers will be high impedance when

VDD is tied to VSS.

3. Function Block Diagram

B54LVDS032LVRH function block diagram is shown in figure 3-1.

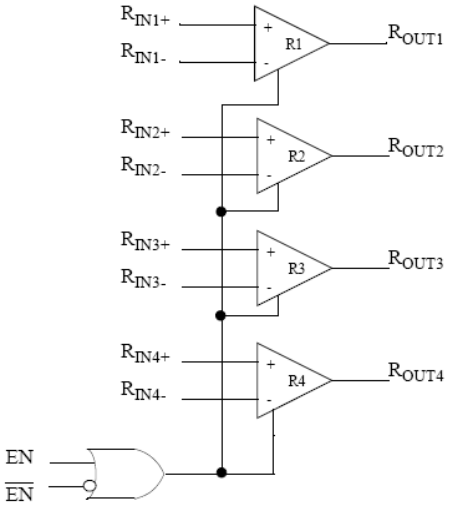


Figure 3-1 B54LVDS032LVRH Quad Driver Block Diagram

4. Packages and Pin Function Descriptions

The provided package is: FP16

B54LVDS032LVRH - pin configuration is shown in 4-1.

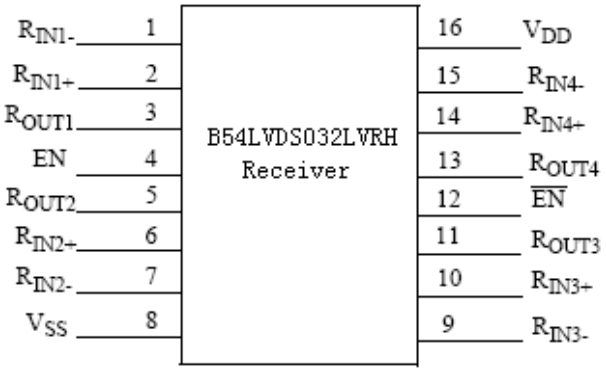


Figure 4-1 B54LVDS032LVRH pin configuration

Table 4-1 B54LVDS032LVRH Pin Function Descriptions

Pin No.	Name	Description
1，7，9，15	R_{IN1}-, R_{IN2}-, R_{IN3}-, R_{IN4}-	Inverting receiver input pin
2，6，10，14	R_{IN1}+, R_{IN2}+, R_{IN3}+, R_{IN4}+	Non-inverting receiver input pin
3，5，11，13	R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4}	Receiver output pin
4	ENABLE	Active high enable pin
12	$\overline{EN}$	Active low enable pin
16	V_{DD}	Power supply pin
8	V_{SS}	Ground pin

5. Pin List

B54LVDS032LVRH pin list is shown in table 5-1.

Table 5-1 B54LVDS032LVRH pin list

Pin No	**Name**	**Description**	**Pin No.**	**Name**	**Description**
1	R_{IN1-}	Inverting receiver input pin	9	R_{IN3-}	Inverting receiver input pin
2	R_{IN1+}	Non-inverting receiver input pin	10	R_{IN3+}	Non-inverting receiver input pin
3	R_{OUT1-}	Receiver output pin	11	R_{OUT3}	Receiver output pin
4	EN	Active high enable pin, OR-ed with EN	12	$\overline{EN}$	Active low enable pin, OR-ed with EN
5	R_{OUT2}	Receiver output pin	13	R_{OUT4}	Receiver output pin
6	R_{IN2+}	Non-inverting receiver input pin	14	R_{IN4+}	Non-inverting receiver input pin
7	R_{IN2-}	Inverting receiver input pin	15	R_{IN4-}	Inverting receiver input pin
8	V_{SS}	Ground pin	16	V_{DD}	Power supply pin, +3.3V ±0.3V

6. Detailed Description

6.1 Truth Table

The B54LVDS032LVRH's. truth table is shown in table 6-1.

Table 6-1 truth table

Enables		Input	Output
EN	$\overline{EN}$	R_{IN+}-R_{IN-}	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H

L = Low logic state

X = Irrelevant

H = High logic state

Z = TRI-STATE (high impedance)

6.2 Timing Diagrams

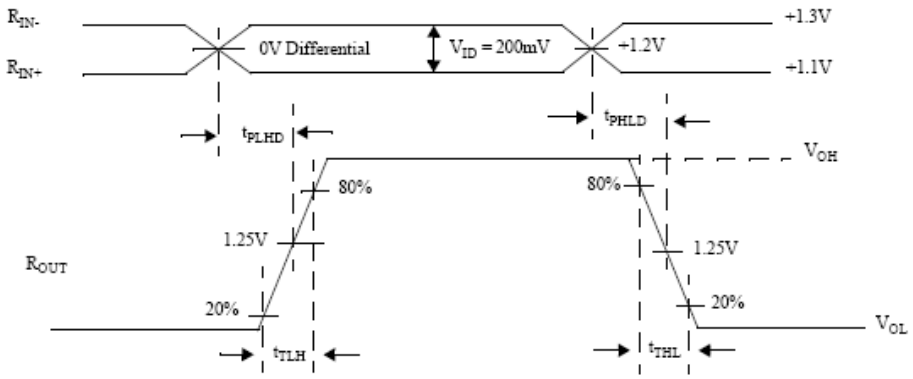


Figure 6-1. Receiver Propagation Delay and Transition Time Waveforms

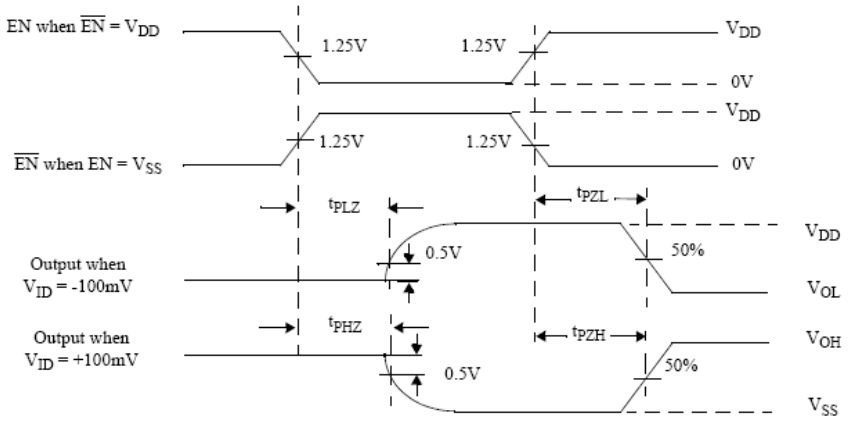


Figure 6-2. Receiver Three-State Delay Waveform

6.3 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 15℃～25℃ and relative humidity less than 65%. There should be no acid , alkali or other radiant gas in the environment.

6.4 Absolute Maximum Ratings

a) Supply voltage range to ground potential(V_{DD})：-0.3V to 4.0 V
b) DC input voltage range(V_{in})：-0.3V to 4.0 V
c) Storage temperature(T_{stg})：-65℃ to +150℃
d) Lead temperature(T_H, 10s)：260℃
e) Junction temperature (T_J)：150℃

6.5 Recommended Operation Conditions

a) Supply voltage relative to ground(VDD)：3.0 V to 3.6 V
b) DC input voltage, receiver inputs ：2.4V
c) DC input voltage, logic inputs：0 to VDD for EN, $\overline{EN}$
d) Case temperature range ：-55℃ to +125℃

7. Specifications

All electrical characteristics are shown in table 7-1，Propagation Delay and Transition Time Waveforms are shown in Figure 7-1，Three-State Delay Waveform is shown in Figure 7-2.

Table 7-1 B54LVDS032LVRH electrical characteristics

DC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	CONDITION (VDD = 3.0V±0.3V; -55℃< TC < +125℃)	LIMITS		UNIT
			MIN	MAX	
High-level input voltage	V_{IH}	（TTL）	2.0	V_{DD}	V
Low-level input voltage	V_{IL}	（TTL）	GND	0.8	V
High-level output voltage	V_{OH}	I_{OH} = -0.4mA, V_{DD} = 3.0V	2.7	—	V
Low-level output voltage	V_{OL}	I_{OL} = 2mA, V_{DD} = 3.0V	—	0.25	V
Logic input leakage current	I_{IN}	VIN = 2.4V	-15	15	μA
		Enables EN/$\overline{EN}$ =0 and 3.6V，V_{DD}=3.6V	-10	10	μA
Cold Spare Leakage LVDS Inputs	I_{CS}	V_{IN}=3.6V，V_{DD}=0V	-20	20	μA
		V_{OUT}=3.6V，V_{DD}=0V			
Differential Input High Threshold	V_{TH}[3]	V_{CM}= +1.2V	—	100	mV
Differential Input Low Threshold	V_{TL}[3]	V_{CM}= +1.2V	-100	—	mV
Input clamp voltage	V_{CL}	I_{CL} = -18 mA	-1.5	—	V
Output Short Circuit Current	I_{OS}[3]	Enabled，V_{OUT}=0V	-130	-15	mA
Output Three-State Current	I_{OZ}[4]	Disabled，EN=0V，$\overline{EN}$=VDD，V_{OUT}=0V or V_{DD}	-10	10	μA
Loaded supply current receivers enabled	I_{CC}[4]	EN=$\overline{EN}$=0V or V_{DD}，IutputS Open	—	15	mA
Loaded supply current receivers disabled	I_{CCZ}[4]	EN=0V，$\overline{EN}$=V_{DD}，IutputS Open	—	7.5	mA

Notes:
1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2. Output short circuit current (IOS) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
3. Guaranteed by characterization.
4. Device tested at VDD=3.0Vand 3.6V.

AC SWITCHING CHARACTERISTICS[1, 2, 3, 4]

PARAMETER	*SYMBOL*	CONDITION (VDD = 3.0V ±0.3V, TA = -55℃ to +125℃)	MIN	MAX	UNIT
Functional Test		f =200MHz， V_{DD}=3.0V			
Differential Propagation Delay High to Low	t_{PHLD}	(figures 6-1 and 7-1)	1.0	4.0	ns
Differential Propagation Delay Low to High	t_{PLHD}	(figures 6-1 and 7-1)	1.0	4.0	ns
Differential Skew (tPHLD - tPLHD)	t_{SKD}		—	350	ps
Channel-to-Channel Skew[1]	t_{SK1}[4]		—	500	ps
Chip-to-Chip Skew[5]	t_{SK2}[4]		—	3.0	ns
Disable Time High to Z	t_{PHZ}[4]	(figures 6-2 and 7-2)	—	12	ns
Disable Time Low to Z	t_{PLZ}[4]	(figures 6-2 and 7-2)	—	12	ns
Enable Time Z to High	t_{PZH}[4]	(figures 6-2 and 7-2)	—	12	ns
Enable Time Z to Low	t_{PZL}[4]	(figures 6-2 and 7-2)	—	12	ns

Notes:
1. Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z0 = 50Ω, tr and tf (0% - 100%) < 1ns for RIN and tr and tf < 6ns for EN or $\overline{EN}$.
3. CL includes probe and jig capacitance.
4. Guaranteed by characterization.
5. Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

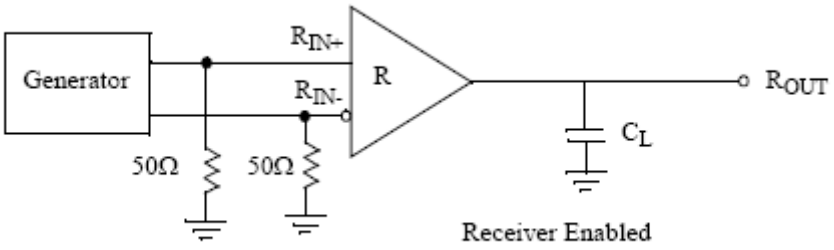


Figure.7-1. Receiver Propagation Delay and Transition Time Test Circuit or Equivalent Circuit

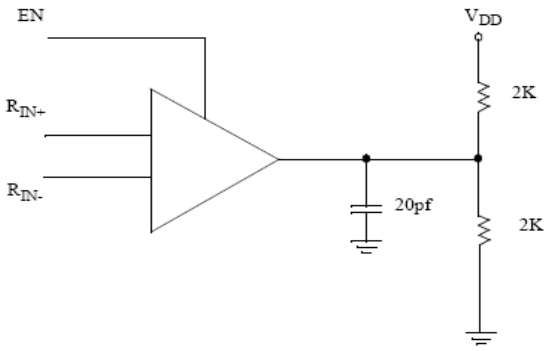


Figure.7-2. Receiver Three-State Delay Test Circuit or Equivalent Circuit

8. Package Specifications

The specifications of FP16 package are shown in figure8-1.

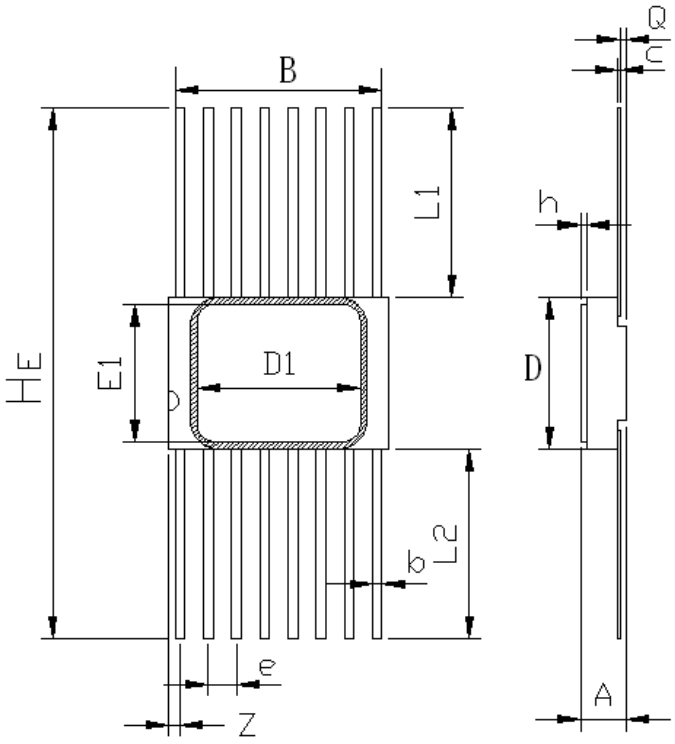


Figure 8-1 FP16 package specifications

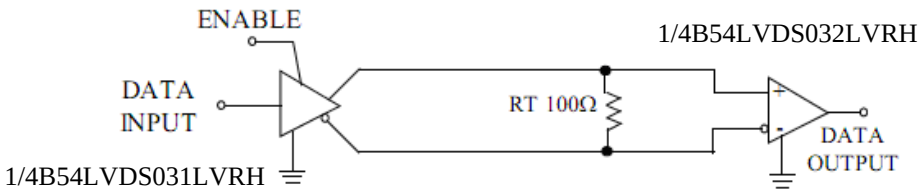
Table 8-1 size symbol list

Symbol	Value（unit：mm）		
	Min	Normal	Max
A	1.60	——	2.50
B	8.94	——	9.69
b	0.25	——	0.54
c	0.07	——	0.20
D	6.55	——	7.25
e	——	1.27	——
He	18.76	19.41	20.06
Q	0.13	——	0.90
L1	5.75	——	6.75
L2	5.75	——	6.75
Z	——	——	1.27
D1	——	7.366	——
E1	——	6.223	——
h	0.22	——	0.28

9. Appendix I Typical Application Example

9.1 Typical Application

The B54LVDS032LVRH receiver's intended use is primarily in an uncomplicated point-to-point configuration as is shown in Appendix figure.9-1. This configuration provides a clean signaling environment for quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into voltages that are detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities, as well as ground shifting, noise margin limits, and total termination loading must be taken into account.



Appendix figure.9-1. Point-to-Point Application

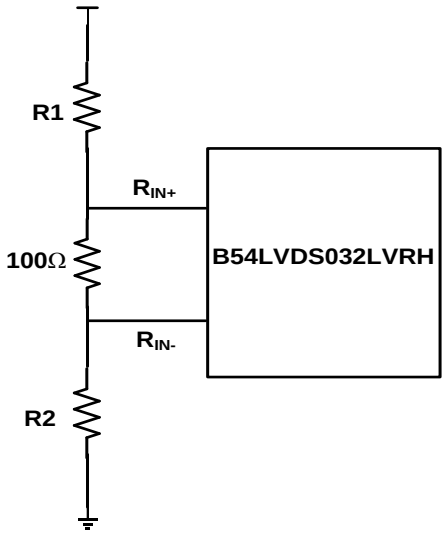
The B54LVDS032LVRH differential line receiver is capable of detecting signals as low as 100mV, over a + 1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift +1V around this center point. The +1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground).

9.2 Cold Spare

All pins have Cold Spare buffers. These buffers will be high impedance when VDD is tied to VSS. But the CMOS outputs (pin 3,5,11,and 14) should not be used as coldspared pins when VDD is not tied to VSS.

9.3 Unused Input

The B54LVDS032LVRH receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to TTL logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal. The B54LVDS032LVRH is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the other unused receivers can be processed with one of ways as follows.



Appendix figure.9-2. B54LVDS032LVRH Termination Application

1. Open Input Pins. The unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

2. Terminated Input. If the driver is disconnected (cable unplugged), or if the driver is in a three-state or power off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins.

The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable offers better balance than flat ribbon cable.

If the unused receivers differential inputs across with 100Ω termination resistor, the positive pin should tie to power with R1(≤7.4K), and the negative pin should tie to ground with R2(≤4.3K) as is shown in Figure 7. The selection of resistance should guarantee the input common voltage around 1.2V.

$$\frac{R2+50}{R1+R2+100}VDD \approx 1.2$$

10. Appendix II Replaced Product

Appendix table.1-1

Device Type	Substituted Device Type
B54LVDS032LVRH	Aeroflex UT54LVDS032LV

Service and Support：

Address： No.2 Siyingmen N. Road. Donggaodi. Fengtai District.Beijing.China.
Department： Department of international cooperation
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