Ver 1.2

Radiation Hardened 3.3V Quad Differential Line Diver

Datasheet

Part Number：B26LV31TERH

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Page of Revise Control

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1. Features

- Single 3.3V Supply
- TTL Inputs
- High Impedance Outputs when Disabled or Powered Down
- EIA RS-422 Compatible Outputs
- Full -55°C to +125°C Military Temperature Range
- Radiation-hardened design：

  Total-dose: 100 krad(Si)

  Latchup immune (LET > 75MeV-cm^2/mg)
- Packaging options:

  16-lead Flatpack
- Low quiescent current

2. General Description

The B26LV31TERH is a quad differential line driver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

3. Function Block Diagram

B26LV31TERH function block diagram is shown in figure 3-1.

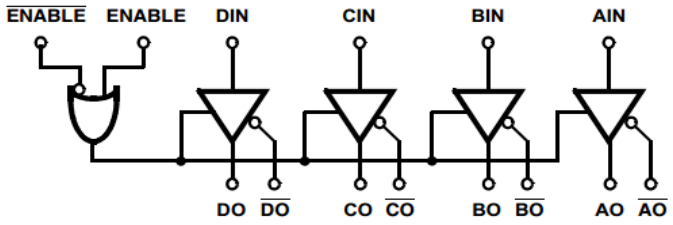


Figure 3-1 B26LV31TERH function block digram

4. Packages and Pin Function Descriptions

The provided package is: FP16.

B26LV31TERH FP16 pin configuration is shown in 4-1.

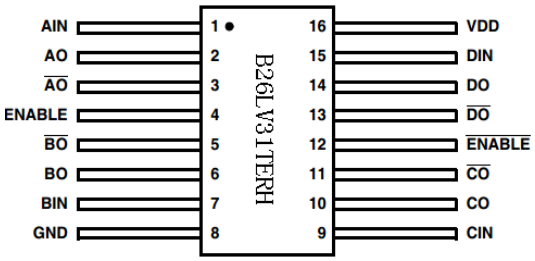


Figure 4-1 FP16 pin configuration

Talble 4-1 B26LV31TERH Pin Function Descriptions

Pin No.	Name	Description
1，7，9，15	AIN,BIN,CIN,DIN	Driver input pin, CMOS compatible
2，6，10，14	AO,BO,CO,DO	Non-inverting driver output pin
3，5，11，13	$\overline{AO}$, $\overline{BO}$, $\overline{CO}$, $\overline{DO}$	Inverting driver output pin
4	ENABLE	Active high enable pin
12	$\overline{ENABLE}$	Active low enable pin
16	VDD	Power supply pin
8	GND	Ground pin

5. Pin List

B26LV31TERH –FP16 pin list is shown in table 5-1.

Table 5-1 B26LV31TERH –FP16 pin list

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	AIN	INPUT DATA1	9	CIN	INPUT DATA3
2	AO	OUTPUT DATA1 POSITIVE	10	CO	OUTPUT DATA3 POSITIVE

3	$\overline{AO}$	OUTPUT DATA1 NEGATIVE	11	$\overline{CO}$	OUTPUT DATA3 NEGATIVE
4	ENABLE	Active high enable pin	12	$\overline{ENABLE}$	Active low enable pin
5	$\overline{BO}$	OUTPUT DATA2 NEGATIVE	13	$\overline{DO}$	OUTPUT DATA4 NEGATIVE
6	BO	OUTPUT DATA2 POSITIVE	14	DO	OUTPUT DATA4 POSITIVE
7	BIN	INPUT DATA2	15	DIN	INPUT DATA4
8	GND	GND	16	VDD	POWER

6. Detailed Description

6.1 Function Description

The B26LV31TERH accepts TTL signal levels and converts them to RS-422 compatible outputs. This circuit uses special outputs that enable the drivers to power-down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independently. truth table is shown in table 6-1.

Table 6-1 truth table

ENABLE	$\overline{ENABLE}$	Input	Non-inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

L = Low logic state

X = Irrelevant

H = High logic state

Z = TRI-STATE (high impedance)

6.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment,

6.3 Absolute Maximum Ratings

a) Supply voltage range to ground potential（V_{DD}）： -0.5V to 7.0 V
b) DC input voltage range（V_{in}）： -0.5V to（V_{DD}+0.5V）
c) DC output voltage (V_{OUT}) power off : -0.5V to 7.0 V
d) Storage temperature（T_{stg}）： -65℃ to 150℃
e) Lead temperature（T_h）： 260℃
f) Junction temperature (TJ)： 150℃

6.4 Recommended Operation Conditions

a) Supply voltage relative to ground（V_{DD}）： 3.0 V to 3.6 V
b) Case operation temperature range(TA) ： -55℃ to 125℃

7. Specifications

All electrical characteristics are shown in table 7-1，Propagation Delay and Transition Time Waveforms are shown in Figure 7-1，Three-State Delay Waveform is shown in Figure 7-2.

Table 7-1 B26LV31TERH electrical characteristics

PARAMETER	SYMBOL	CONDITION	LIMIT		UNIT
		（-55℃≤ TA ≤ 125℃ ，3.0V≤V_{DD}≤ 3.6V）unless otherwise specified	MIN	MAX	
High-level input voltage	V_{IH}	V_{DD}=3.0V，3.6V	2.0	—	V
Low-level input voltage	V_{IL}	V_{DD}=3.0V，3.6V	—	0.8	V
Low level input current	I_{IL}	V_{IN}= 0V，V_{DD}=3.6V	-10	—	μA

PARAMETER	SYMBOL	CONDITION	LIMIT		UNIT
		（-55℃≤ TA ≤ 125℃ ，3.0V≤V_{DD}≤ 3.6V） unless otherwise specified	MIN	MAX	
High level input current	I_{IH}	V_{IN}= 3.6V， V_{DD}=3.6V	—	10	μA
Differential Output Voltage	V_{OD1}	V_{DD}=3.0V/3.6V,R_L=no load	—	4.0	V
	V_{OD2}	V_{DD}=3.0V/3.6V,R_L=100Ω	2.0	—	V
	V_{OD3}	V_{DD}=3.0V/3.6V,R_L=3900Ω	—	3.6	V
Difference in differential output	$V_{OD2} - \overline{V_{OD2}}$	V_{DD}=3.0V/3.6V,R_L=100Ω	-0.4	0.4	V
Common mode output voltage	V_{OC}	V_{DD}=3.0V/3.6V,R_L=100Ω	—	2.0	V
Difference in common mode output voltage	$V_{OC} - \overline{V_{OC}}$	V_{DD}=3.0V/3.6V,R_L=100Ω	-0.4	0.4	V
Input clamp voltage	V_{C1}	I_{IN} =-18 mA， V_{DD}=3.0V	-1.5	—	V
Output Short Circuit Current[1/]	I_{SC}	V_{IN}=V_{DD},V_{OUT}=0V and V_{IN}=0V,V_{OUT}=0V	-30	-160	mA
Output Three-State Current	I_{OZ}	V_{DD}=3.6V, ENABLE=0V ，$\overline{ENABLE}$ =3.6V， V_{OUT}=V_{DD} or GND	-20	20	μA
Standby supply current	I_{CC}	V_{DD}=3.6V, VIN=V_{DD} and GND IO =0μA	—	125	uA
Output leakage current power OFF	Ioff	V_{DD}=0V, V_{OUT}=6V,3 V	—	100	uA
		V_{DD}=0V, V_{OUT}=-250mV	-200	—	uA
Function test	FT	f =10MHz			
Differential Propagation Delay High to Low[2/]	t_{PHLD}	V_{DD}=3.0V R_L=100Ω C_L=50p Figure 7-1	5	25	ns
Differential Propagation Delay Low to High[2/]	t_{PLHD}	V_{DD}=3.0V R_L=100Ω C_L=50p Figure 7-1	5	25	ns

PARAMETER	SYMBOL	CONDITION （-55℃≤ TA ≤ 125℃ ， 3.0V≤V_{DD}≤ 3.6V） unless otherwise specified	LIMIT		UNIT
			MIN	MAX	
Differential skew tPHLD-tPLHD (same channel) 2/	t_{SKD}	V_{DD}=3.0V R_L=100Ω C_L=50p Figure 3	—	5	ns
Pin to pin skew (same device)2/	t_{SK1}	V_{DD}=3.0V R_L=100Ω C_L=50p Figure 7-1	—	5	ns
Disable Time High to Z3/	t_{PHZ}	V_{DD}=3.0V R_L=110Ω to GND C_L=50p ,Figure 7-2	—	35	ns
Disable Time Low to Z3/	t_{PLZ}	V_{DD}=3.0V R_L=110Ω to V_{DD} C_L=50p,Figure 7-2	—	35	ns
Enable Time Z to High3/	t_{PZH}	V_{DD}=3.0V R_L=110Ω to GND C_L=50p ,Figure 7-2	—	40	ns
Enable Time Z to Low3/	t_{PZL}	V_{DD}=3.0V R_L=110Ω to V_{DD} C_L=50p,Figure 7-2	—	40	ns

1/ Only one output at a time may be shorted.

2/ Generator waveform is specified as follows: f = 1 MHz, duty cycle = 50% tr = tf ≤ 6 ns. Driver input = 0 V to 3 V with measure points equal to 1.5 V. Differential output V_{DIFF} with measure point equal to 0 V.

3/ Generator waveform is specified as follows: f = 1 MHz, duty cycle = 50%, tr = tf ≤ 6 ns. ENABLE/ $\overline{\text{ENABLE}}$ inputs 0 V to 3 V with measure points equal to 1.5 V on the inputs, to 1.3 V on the outputs for ZL and ZH, and (V_{OL} + 0.3 V) for LZ, and(V_{OH} – 0.3 V) for H_Z.

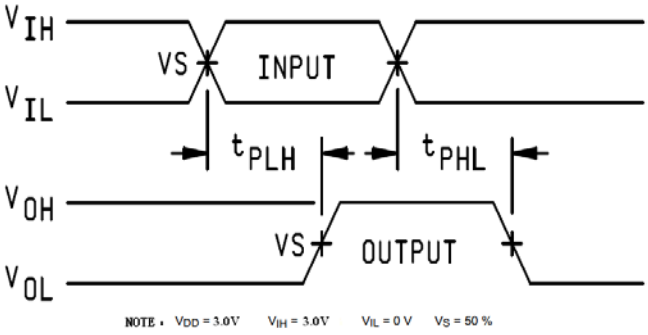


Figure.7-1. Driver Propagation Delay and Transition Time Waveforms

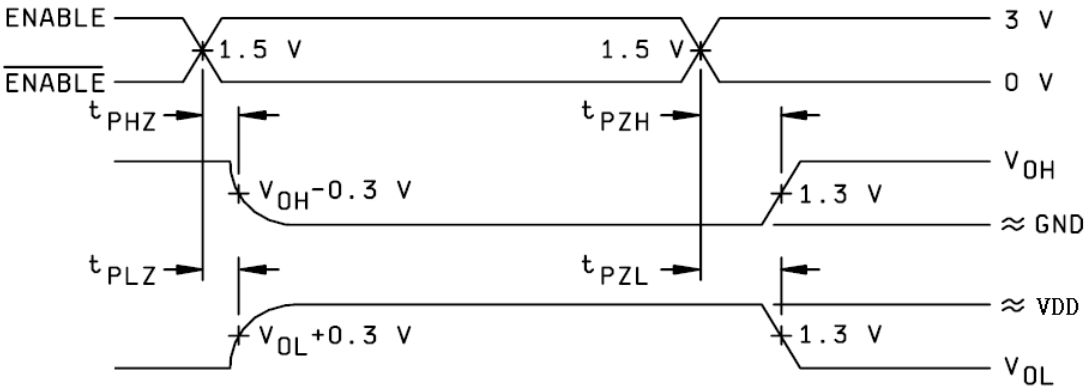


Figure.7-2. Driver Three-State Delay Waveform

8. Package Specifications

The specifications of FP16 package are shown in figure8-1.

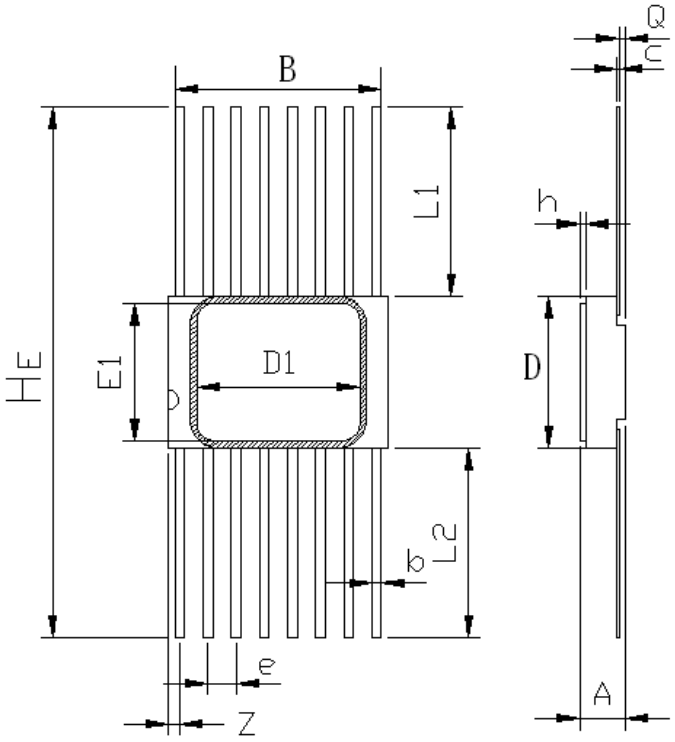


Figure 8-1 FP16 package specifications

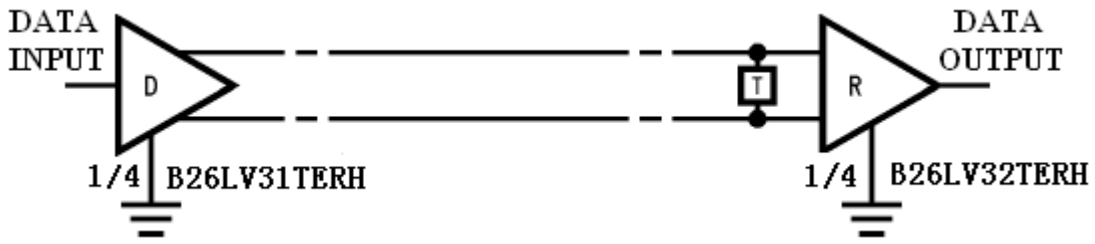
Table 8-1 size symbol list

Symbol	Value（unit：mm）		
	Min	Normal	Max

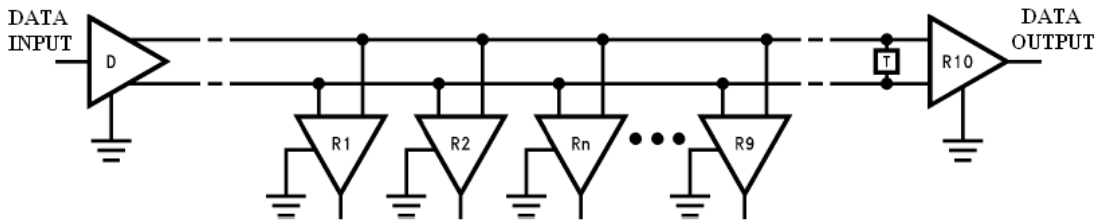
A	1.60	——	2.50
B	8.94	——	9.69
b	0.25	——	0.54
c	0.07	——	0.20
D	6.55	——	7.25
e	——	1.27	——
He	18.76	19.41	20.06
Q	0.13	——	0.90
L1	5.75	——	6.75
L2	5.75	——	6.75
Z	——	——	1.27
D1	——	7.366	——
E1	——	6.223	——
h	0.22	——	0.28

9. Appendix I Typical Application Example

The B26LV31TERH driver's intended use is primarily in an uncomplicated point-to-point configuration as is shown in Appendix figure.1-1. This configuration provides a clean signaling environment for quick edge rates of the drivers. The receiver is connected to the driver through a balanced media such as a standard twisted pair cable. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media and is located as close to the receiver input pins as possible. Other configurations are possible such as a multireceiver configuration, Multidrop configuration as is shown in Appendix figure.1-2.



Appendix figure.1-1. Point-to-Point Application



Appendix figure.1-2. Multidrop Application

10. Appendix II Replaced Product

Appendix table.1-1

Device Type	Substituted Device Type
B26LV31TERH	NSC DS26LV31QML

Service and Support：

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